

Aalborg Universitet



AALBORG UNIVERSITY
DENMARK

Reliability Oriented Circuit Design For Power Electronics Applications

Sintamarean, Nicolae Cristian

Publication date:
2015

Document Version
Publisher's PDF, also known as Version of record

[Link to publication from Aalborg University](#)

Citation for published version (APA):
Sintamarean, N. C. (2015). *Reliability Oriented Circuit Design For Power Electronics Applications*. Department of Energy Technology, Aalborg University.

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

Take down policy

If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

Reliability Oriented Circuit Design For Power Electronics Applications

By

Nicolae-Cristian Sintamarean



DEPARTMENT OF ENERGY TECHNOLOGY
AALBORG UNIVERSITY

Center of Reliable Power Electronics (CORPE)

Dissertation Submitted to

The Faculty of Engineering and Science, Aalborg University in
Partial Fulfilment for the Degree of Doctor of Philosophy

January 2015

Aalborg, Denmark

Aalborg University
Department of Energy Technology
Pontoppidanstræde 101
9220 Aalborg East
Denmark
Phone: +45 9940 9240
Fax: +45 9815 1411
Web: <http://www.et.aau.dk>
Copyright © Nicolae-Cristian Sintamarean, 2015
Printed in Denmark by UniPrint
ISBN: 978-87-92846-52-5

Copyright Statement

Thesis title: Reliability Oriented Circuit Design for Power Electronics Applications

Name of the PhD student: Nicolae-Cristian Sintamarean

Name of supervisors: Prof. Frede Blaabjerg

List of publication: Listed in § 1.7

This present report combined with scientific papers which are listed in § 1.7 has been submitted to the Faculty of Engineering and Science at Aalborg University for assessment in partial fulfillment for the Degree of Doctor of Philosophy (Ph.D.) in Electrical Engineering. The scientific papers are not included in this version due to copyright issues. Detailed publication information is provided in § 1.7 and the interested reader is referred to the original published papers. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University.

Preface

The submission of this thesis marks the end of a wonderful period from 1st September 2012 to 31st January 2015 in which I was a PhD student in the Department of Energy Technology at Aalborg University. The PhD period has been the most challenging experience encountered yet and I wish to express my deepest gratitude to those who gave me the strength and courage to evolve and move forward.

First of all, I am extremely grateful to my supervisor from Aalborg University Professor Frede Blaabjerg, to Professor Francesco Iannuzzo and to Assistant Professor Huai Wang. Their valuable guidance and professional support made my PhD experience challenging and productive.

Many thanks to my colleagues from the Department of Energy Technology for their friendly guidance and support. In particular, I thank to Bogdan Craciun, Catalin Dancan, Emanuel Eni and Cam Pham for their caring support and warm encouragements.

I am deeply thankful to my parents for their unconditional love and continuous support. And last, but not least, I also dedicate this thesis to my loving fiancé Iulia. Without her priceless advices none of my achievements would have been possible.

Nicolae-Cristian Sintamarean
January 2015, Aalborg

Abstract

Highly reliable components are required in order to minimize the downtime during the lifetime of the converter and implicitly the maintenance costs. Therefore, the design of high reliable converters under constrained reliability and cost is a great challenge to be overcome in the future. The temperature variation of the semiconductor devices plays a key role in the robustness design and reliability of power electronics converters. This factor has a major impact on the power converters used in renewable energy systems, like solar and wind energy applications, due to the fluctuating nature of the mission profile. The mission profile variations introduce converter current changes which further cause device junction temperature variations that significantly reduce the reliability of the semiconductor devices. Therefore, in order to achieve reliability improvement and cost reduction of the renewable energy technology, a reliability-oriented design tool is of great interest. This tool is expected to perform the long-term (e.g. one year) electro-thermal and then the reliability aspect analysis of the switching devices in the new generation of power converters. Besides this, another important method for improving the reliability is by active thermal control of the power electronic devices.

The work developed during the Ph.D. studies the above mentioned topics, and is divided into two main parts: the first part develops a reliability-oriented design tool which is using a long term real-field mission-profile as input and the second part propose an advanced gate-driver concept for enhancing the reliability of the power electronics devices. Chapter 1 introduce the emerging challenges of a design tool for reliability and which are the main methods for achieving active thermal control of the devices. To overcome the emerging challenges described in Chapter 1, the first part of the thesis focuses on the proposed reliability tool and it is presented in Chapter 2 and Chapter 3. In this part is introduced a novel concept of assessing the reliability of power semiconductor devices by considering the device degradation and the mission profile operating conditions. The detailed modeling process of the tool is presented in Chapter 2. Afterwards the translation process

from the Detailed Simulation Model (DSM) to the Long Term Simulation Model (LTSM) in order to consider the mission profile impact on device thermal loading is presented.

Chapter 3 presents the electro-thermal model validation and the reliability studies performed by the proposed tool. The chapter ends with a detailed lifetime analysis, which emphasizes the mission-profile variation and gate-driver parameters variation impact on the PV-inverter devices lifetime. Moreover, the impact of the mission-profile sampling time on the lifetime estimation accuracy is also determined.

The second part of the thesis introduced in Chapter 4, presents a novel gate-driver concept which reduces the dependency of the device power losses variations on the device loading variations. The proposed gate-driver is able dynamically and accurately to control the gate-resistance and gate-voltage in order to preserve constant the device losses dissipation, implicitly also the device temperature. In order to proof the concept, the hardware implementation of the proposed active thermal control has been done. The chapter ends with a detailed lifetime analysis, which emphasizes the mission profile variation and advanced gate-driver strategy impact on the converter device lifetime.

The main contribution of this project is in developing of a novel reliability oriented design tool for the next generation of power converters. The tool introduces a novel concept of assessing the reliability of power semiconductor devices by considering the device degradation related to the real field operating conditions. Moreover, the project it also introduces a novel gate-driver concept which reduces the dependency of the device power losses (implicitly temperature) variations on the device loading variations, enhancing the reliability of power electronics devices.

Dansk resumé

Meget pålidelige komponenter er nødvendige for at minimere fejl niveauet under konverterens levetid, inklusiv vedligeholdelsesomkostninger. Derfor, designet af høj pålidelige omformere under begrænset pålidelighed og omkostningerne er en stor udfordring, der skal overvindes i fremtiden. Semiconductorernes temperatur variation spiller en central rolle i robustheds design og pålidelighed af effektelektronik omformere. Denne faktor har stor indflydelse på strøm omformere, der bruges i vedvarende energisystemer, ligesom sol- og vindenergi applikationer, på grund af den svingende karakter af missionens profil. Missionens profil variationer indfører aktuelle forandringer i konverteren, som yderligere forårsager enhed junction temperatur variationer (på grund af strømsvigt dissipation), som reducerer semiconductor komponenternes pålidelighed.

Derfor, for at kunne opnå pålidelighedens forbedring og omkostningsreduktion af vedvarende energi teknologi, en pålidelighed-orienteret design værktøj er af stor interesse. Dette værktøj forventes til at udføre langsigtede (fx et år) elektro-termiske og derefter pålidelighedens analyse af skiftende enheder i den nye generation af el-konvertere. Ud over dette, en anden vigtig metode til at forbedre pålidelighed opnås ved aktiv termisk styring af enhederne.

Arbejdet udført under Ph.D. uddannelsen dækker ovennævnte emner, og er opdelt i to hoveddele: den første del udvikler en pålidelighed-orienteret design værktøj, der bruger en langsigtet real-felt mission-profil som input og den anden del foreslå et avanceret gate-driver koncept til forbedring af effektelektronik udstyrens pålidelighed. Kapitel 1 indfører de nye udfordringer i et design værktøj til pålidelighed (baseret på en real-felt mission profil), og hvad er de vigtigste metoder til at opnå udstyrets aktive termisk kontrol. For at overvinde de nye udfordringer, der er beskrevet i kapitel 1, fokuserer den første del af afhandlingen på den foreslåede pålidelighed værktøj, og det er præsenteret i kapitel 2 og kapitel 3. I denne del er der indført et nyt koncept til at vurdere pålideligheden af power semiconductor komponenter, ved at betragte enhedens nedbrydning og mission-profilens driftsbetingelser. Værktøjets

detaljerede modellering er præsenteret i kapitel 2. Herefter præsenteres oversættelsesprocessen fra den detaljerede Simulation Model (DSM) til Long Term Simulation Model (LTSM), for at overveje mission profilens indvirkning på enhedens termisk lastning.

Kapitel 3 præsenterer den elektro-termiske model validering og pålidelighed undersøgelser, udførte af det foreslåede værktøj. Kapitlet slutter med en detaljeret levetid analyse, som fremhæver mission-profilens variation og gate-driver parametre variationens indvirkning på PV-inverters levetid. Desuden, afgøres der også missionens profil samplings tids effekt over levetidens estimerings nøjagtighed.

Den anden del af afhandlingen, introduceret i kapitel 4, præsenterer en ny gate-driver koncept som reducerer enhedens power tab variationernes afhængighed af enhedens lastning variationer. Den foreslåede gate-driver er i stand, dynamisk og præcist, til at kontrollere gate-modstand og gate-spænding med henblik på at bevare stabiliteten i enhedens tab dissipation, og implicit enhedens temperatur. For at bevise konceptet, blev der udført en hardware gennemførelse af den foreslåede aktive termiske kontrol. Kapitlet slutter af med en detaljeret levetid analyse, som fremhæver mission profilens variationer og avanceret gate-driver strategiens indvirkning på konverterens levetid.

Dette projekts vigtigste bidrag er udviklingen af et hidtil ukendt pålidelighed-orienteret design værktøj til den næste generation af omformere. Værktøjet introducerer et nyt koncept, til at kunne vurdere power semiconductorernes pålidelighed, ved at overveje enhedens nedbrydning i forhold til de reelle felt driftsbetingelser.

Desuden projektet indfører også en ny gate-driver koncept, der reducerer enhedens strøm tab variationernes afhængighed (implicit temperatur) af enhedens lastning variationer, som forbedrer effektelektronik udstyrens pålidelighed.

Table of contents

Preface.....	i
Abstract.....	iii
Dansk resumé	v
Table of contents	vii
Nomenclature	ix
PART I – Report	1
Chapter 1 Introduction.....	1
1.1 Saturation of Silicon-based devices	1
1.2 The impact of Wide Band-Gap semiconductors in power electronic devices development	3
1.3 Evolution and maturing of the Silicon-Carbide devices technology	6
1.4 Emerging challenges of a design tool for reliability	9
1.4.1 <i>Mission Profile importance in reliability.....</i>	<i>10</i>
1.4.2 <i>Translation of the long-term Mission-Profile to device-level thermal loading.....</i>	<i>12</i>
1.5 Project objectives	15
1.6 Thesis outline	16
1.7 List of publications.....	18
Chapter 2 Mission-Profile Reliability-Oriented Design Tool.....	21
2.1 Real Field Mission Profile model	23
2.2 Grid-Connected PV-inverter Model.....	24
2.3 Electro-Thermal Model.....	27
2.3.1 <i>Device model.....</i>	<i>29</i>
2.3.2 <i>Thermal model</i>	<i>35</i>
2.4 Device Lifetime Model	39
2.5 Translation from Detailed Simulation Model to Long Term Simulation Model.....	42
2.6 Summary	47
Chapter 3 Model Validation and Lifetime Analysis of SiC-based PV-inverter Devices	49
3.1 SiC-based PV-inverter selection	49
3.1.1 <i>PV-inverter complexity</i>	<i>50</i>
3.1.2 <i>Thermal loading comparison of the selected topologies.....</i>	<i>52</i>

3.1.3	<i>Cost rentability of the selected SiC-based PV-inverter.....</i>	<i>55</i>
3.2	Electro-Thermal model validation.....	57
3.2.1	<i>Device level validation</i>	<i>57</i>
3.2.2	<i>Electro-thermal model validation for converter level operation.....</i>	<i>60</i>
3.3	Lifetime analysis of SiC-based PV-inverter devices	62
3.3.1	<i>The impact of Mission-Profile variation from soft to harsh operating conditions.....</i>	<i>62</i>
3.3.2	<i>The impact of Gate-Driver parameters variation.....</i>	<i>66</i>
3.3.3	<i>The impact of Mission-Profile sampling-time in the lifetime estimation accuracy.....</i>	<i>67</i>
3.4	Summary.....	69
Chapter 4 A Novel Gate-Driver Concept for Enhancing the Reliability of Power-Semiconductor Devices		71
4.1	Advanced Gate-Driver concept	72
4.2	Proposed Advanced Gate-Driver circuit for temperature control of power-devices	75
4.2.1	<i>Active gate-voltage (V_G) control</i>	<i>76</i>
4.2.2	<i>Active gate-resistance (R_G) control</i>	<i>76</i>
4.3	The device active-thermal control based on the Advanced Gate-Driver concept	77
4.4	Advanced Gate-Driver validation.....	81
4.5	Advanced Gate-Driver strategy impact in reliability of the PV-inverter devices	83
4.6	Summary.....	86
Chapter 5 Conclusions and Future Work		87
5.1	Summary of Conclusions.....	87
5.2	Contributions from the Authors Point of View	89
5.3	Future work.....	90
Bibliography.....		91
PART II - Publications.....		99
Publication I.....		101
Publication II		111
Publication III.....		119
Publication IV		131
Publication V.....		143
Publication VI		151
Publication VII.....		161
Publication VIII.....		171

Nomenclature

ΔT_{ca}	– case-to-ambient temperature drop
ΔT_{jc}	– junction-to-case temperature drop
ΔT_j	– junction temperature variation,
2L, 3L	– two level, three level,
2L-FB	– two level full bridge,
3L-BS NPC	– three level bipolar switch neutral point clamping
3L-DNPC	– three level diode neutral point clamping,
AGD	– advanced gate-driver,
ar	– wire bond aspect ratio,
A	– technology factor,
a	– temperature coefficient
C_{GD}	– gate-drain capacitance
C_{ISS}	– input capacitance
CTE	– thermal expansion coefficient
C_{th}	– thermal capacitance
D	– device degradation
Dy	– duty-cycle
DPT	– double-pulse tester
E_a	– activation energy
E_{on}	– turn-on switching energies
E_{off}	– turn-off switching energies
d_{Diode}	– diode chip thickness
f_{SW}	– switching frequency of the device
G	– solar irradiance
GaN	– gallium nitride
GD	– gate driver
GTO	– gate turn-on thyristor
HVDC	– high voltage dc
I_c	– converter output current
I_D	– freewheeling diode current
I_G	– gate current
IGBT	– insulated gate bipolar transistor
I_M	– MOSFET drain current
I_s	– saturation current

JFET	– junction field effect transistor
k	– Boltzmann constant
LT	– lookup table
LTSM	– long term simulation model
MOSFET	– metal-oxide semiconductor field effect transistor
MP	– mission profile
MPPT	– maximum power point tracking
n	– correction coefficient for improving the estimation accuracy
N_f	– number of cycles to failure
P_B	– blocking losses
P_C	– conduction losses
P_{sw}	– switching losses
PCB	– printed circuit board
P_{L-MOS}	– device power loss
$P_{L-Total}$	– total converter power loss,
P_{tot_loss}	– total power losses
Q_{GD}	– gate-drain charge
Q_{rr}	– reverse recovery charge of the diode
Q	– the elementary charge
RFMP	– real field mission profile
R_G	– gate resistance
ROD-tool	– reliability oriented design tool
R_{on}	– device on-state resistance,
R_{th_jc}	– junction-to-case thermal resistance
Si	– silicon
SiC	– Silicon carbide
SOA	– safe operating area
T_a	– ambient temperature
T_c	– device case temperature
T_J	– device junction temperature
t_{fi}	– falling time of the current
t_{fv}	– falling time of the voltage
TGD	– traditional gate-driver
t_{on}	– load pulse duration
t_{ri}	– rise time of the current
t_{rv}	– rise time of the voltage
T_s	– sampling time
T_{sw}	– switching period
V_{DC}	– device off-state voltage

$V_{\text{DC-Link}}$	– DC-Link voltage
V_{DD}	– device blocking voltage
V_{DS}	– MOSFET on-state voltage-drop
V_{F}	– diode forward voltage-drop
V_{G}	– gate-source voltage
V_{pl}	– plateau voltage
VSI	– voltage source inverter
V_{th}	– threshold voltage
V_{Th}	– device thermal voltage
WBG	– wide band-gap
$Z_{\text{th_jc}}$	– device junction-to-case thermal impedance
$Z_{\text{th_ch}}$	– thermal grease thermal impedance
$Z_{\text{th_ha}}$	– heatsink thermal impedance

PART I – Report

Chapter 1

Introduction

This chapter presents the background, motivation and problem formulation of the PhD thesis. It continues with the main objectives and ends with a list of the main scientific contributions above the state-of-the-art brought through this project.

1.1 Saturation of Silicon-based devices

Nowadays, more than 70% of electricity is processed by power electronics. The main users of power-electronics devices are the industrial consumers, the power producer companies and the home appliances [1]. Due to the electronics evolution, every year the price of electronic components has a downward trend favoring their use in all branches [2]. The history of modern power-electronics started in the middle of the last century, once with the invention of the bipolar junction transistor. Furthermore in 1960s, the thyristor was the first device used in power electronics applications. The evolution continued according to Figure 1-1 where it can be clearly seen the most important devices which majorly contributed to the power electronics history development [2].

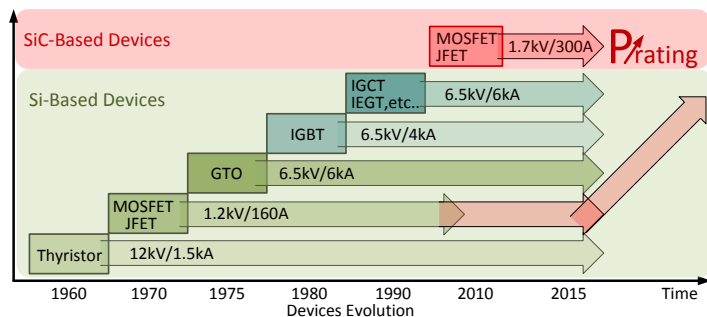


Figure 1-1 Time evolution of power electronics devices

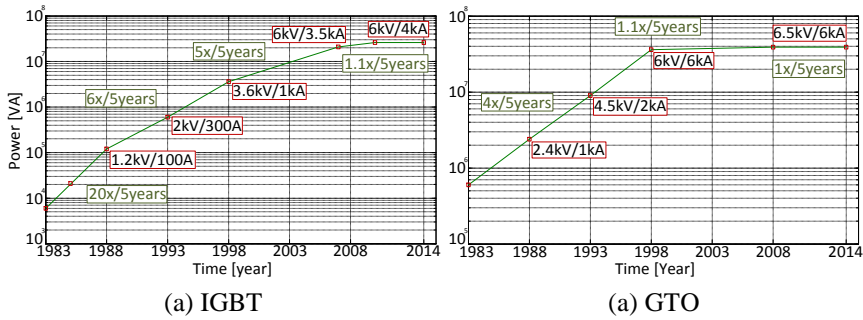


Figure 1-2 The advance in power handling capacity of (a) IGBT and (b) GTO

The improvement of power electronic systems is directly related with the evolution of power semiconductor devices. Silicon (Si)-based semiconductor technology has been highly developed during the last half century. Nowadays, it is hard to achieve any breakthrough of the Si-devices. The main objectives of research and manufacturing are to integrate and perfect the features and characteristics of the existing Si-devices. As an example the IGBTs and GTOs have not been significantly improved in terms of power rating in the last decade. [3]

According to Figure 1-2(a) the power handling of IGBTs increased initially with a rate of 20 times every 5 years. Around 2005, the rate of growth diminished to approximately 5 times every 5 years. Lately, no significant increase could be seen in the last 5 years. A similar evolution occurred with GTOs where Figure 1-2(b) shows that the last 15 years has not brought any significant improvement in power handling capacity [3].

Nowadays, the development of silicon (Si) semiconductor technology has almost achieved its theoretical maturity, exploiting through the maximum physical limits the silicon material. Silicon power devices cannot handle the current market demands in terms of high power device requirements for some applications. [4]

In high voltage applications, for example the HVDC stations, stacking of packaged devices in series are required (e.g. GTOs and thyristors) in order to face the breakdown voltage requirements. Series stacking device connection, is expensive from a packaging point of view, and involves a complicated design in order to avoid uneven voltage-sharing between the devices in the stack.

This problem can also be seen in low power applications, which are strongly influenced by the efficiency. For example to increase the

efficiency of PV-systems, most of solutions for PV-inverters have moved to three-level (3L) structures (this involves the series connection of the devices) reaching high efficiencies (of +96 %) due to low switching losses of 600V Si IGBT or MOSFET and reduced core losses in the output filter [5, 6]. Hence there is a strong incentive to develop devices having greater voltage blocking capabilities, higher efficiency, higher switching frequency, higher power density, higher reliability and lower cost. In this context, the development of power electronics devices based on Wide Band-Gap (WBG) semiconductors, like Silicon Carbide (SiC) and Gallium Nitride (GaN), are interesting. Modern power electronics devices become more demanding by going beyond the capabilities offered by the silicon devices [2].

1.2 The impact of Wide Band-Gap semiconductors in power electronic devices development

A semiconductor material with superior electro-thermal properties (compared with Si) is required in order to build the next generation of high power devices. In this context, the development of power electronics devices based on Wide Band-Gap (WBG) semiconductors is of great interest and has been seen as a potential in the past 20 years. The following table presents some of the most used WBG-semiconductor materials and their main characteristics in comparison with Si material:

Table 1-1 Physical characteristics of Si and the major WBG semiconductors [7]

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap E_g [eV]	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant ϵ_r	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field E_c [kV/cm]	300	400	2500	2200	2000	10000
Electron mobility μ_n [cm ² /V·s]	1500	8500	500 80	1000	1250	2200
Hole mobility μ_p [cm ² /V·s]	600	400	101	115	850	850
Thermal conductivity λ [W/cm·K]	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity v_{sat} [x10 ⁷ cm/s]	1	1	2	2	2.2	2.7

By considering the above table, the main advantages of WBG-devices in comparison with the Si based ones are as follows [2][4][7]:

- The maximum operational temperature of a semiconductor material is determined by the bandgap. Therefore, semiconductors with wider bandgap can operate at higher temperatures. The maximum allowed operating temperature for each semiconductor can be estimated by assuming a maximum of 150°C for Si and multiplying this temperature by the bandgap ratio in respect to that of Si as suggested by [2]. Therefore, the 6H-SiC, 4H-SiC and GaN have similar value, all above 400°C, and the diamond of 730°C, which is much higher than 150°C for Si. WBG-devices can operate at higher temperature levels without losing their electrical characteristics. Therefore they can perform well in extreme conditions, where Si devices cannot be used.
- A higher breakdown voltage is achieved due to the higher electric breakdown field of the WBG-semiconductor. Assuming the same doping density, the theoretical breakdown voltage of a diamond, 6H/4H-SiC and GaN is 514, 56/46 and 34 times higher than Si used in diode [2]. Moreover with higher electric breakdown field, higher doping concentration can be applied to the material. Therefore, the width of the device drift region is reduced when compared to Si. Thus Si requires around 10 times thicker drift region (which imply 10 times higher on-resistance) than SiC and GaN devices for the same blocking voltage capability. This results in WBG-devices with lower on-resistance, which gives lower conduction losses.
- Higher thermal conductivity of the material has a positive impact on the heat distribution among the semiconductor chip surroundings, thus the device junction temperature increases more slowly. This property is very important in high-power, high temperature operation because the heat generated inside the device needs to be dissipated as fast as possible. Moreover, a higher power density of the devices may also be achieved. As it can be seen in Table 1-1, GaN has the lowest thermal conductivity among the semiconductors, even worse than Si. Therefore most research of GaN is focused on low power devices and of SiC on high power devices.

- Another important parameter which influences the performance of semiconductor material in terms of switching frequency speed capability is the high saturation drift velocity. This (the higher drift velocity) allows the charges in the depletion region of a device to be removed faster, resulting in short reverse recovery time. The drift velocity of WBG-semiconductors is more than twice than the one of Si. Therefore, the WBG devices could be switched at higher frequencies than their Si counterparts. This results in devices with lower switching losses.

Even though WBG-devices have the above mentioned advantages, (when compared to Si-based ones) there are some challenges which have to be overpassed in order to take fully advantage of this semiconductor material [8, 9]:

- The WBG-semiconductor inside the device cannot be exploited through its rated limits due to the present unavailability of high temperature packaging techniques which now are in the process of being developed. To understand the fully potential of this material it is worth to mention that the device may require a packaging with performances of a power density of 1000 W/cm^2 and a temperature of $300 \text{ }^\circ\text{C}$ or more. Meanwhile, the currently available packaging technique has a power density of 280 W/cm^2 and a maximum allowed temperature of less than $125 \text{ }^\circ\text{C}$ [8].
- High power devices require larger die size ($>1 \text{ cm}^2$ for megawatt switching), low defect density and large diameter wafers for higher yield in order to lower the costs. The commercialization of SiC-devices has been limited due to the high density of defects as: micropipes, dislocations, misoriented blocks, mosaicity, strain, intrinsic point defects, and foreign polytype inclusions [2]. The main obstacle for growing viable wafers are the micropipes. This determines the price increase of SiC-devices as it gives a lower yield. Currently the price of SiC is 2-4 times higher than Si devices. As shown in Figure 1-3, 50% of the total cost of SiC devices comes from the process, 40% from SiC-material, and 10% from the packaging and testing [9]. Thus SiC material and processing technology are critical factors, which dominates the cost of SiC devices and influence their prospects in the future market.

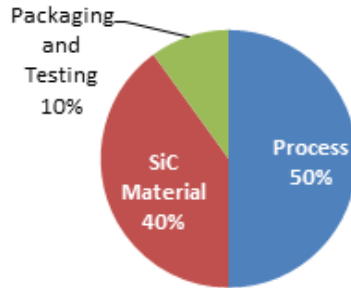


Figure 1-3 Typical cost breakdown of SiC-device technology [9]

1.3 Evolution and maturing of the Silicon-Carbide devices technology

Even since 1950's it was announced that the SiC-semiconductor will be used in the next generation of power electronics devices once Si material will be exploited through its physical limits [10]. Their recent commercialization is expected to revolutionize the power electronics industry in the near future. When discussing the technology maturity it can be stated that the cost reduction of the SiC industry is directly related with the evolution of the SiC-wafers. As it can be seen in Figure 1-4, there are mainly three wafer evolution stages from 75 mm in 2001, 100 mm in 2005 to 150 mm in 2012. The wafer development dramatically reduced the defect densities having a positive impact in the cost reduction of SiC technology [11]. As shown in Figure 1-4, when compared the price of the last generation of produced SiC devices with the first generation, a significant improvement in price reduction has been achieved over the past years due to wafer industry evolution [12].

In 2001 the diode was the first SiC commercially available device. Nowadays, the SiC diode has reached the 5th generation with a 5 times lower cost when compared to first generation. The SiC diode industry is continuing to mature rapidly. Nowadays there are over 100 different SiC diode part numbers available on the market with a breakdown voltage from 600 V to 1.7 kV and current ratings from 1 A to 100 A. The main producers are CREE, Infineon and Rohm. In 2011, the SiC industry achieved a major milestone as the first commercial SiC MOSFETs were released [13].

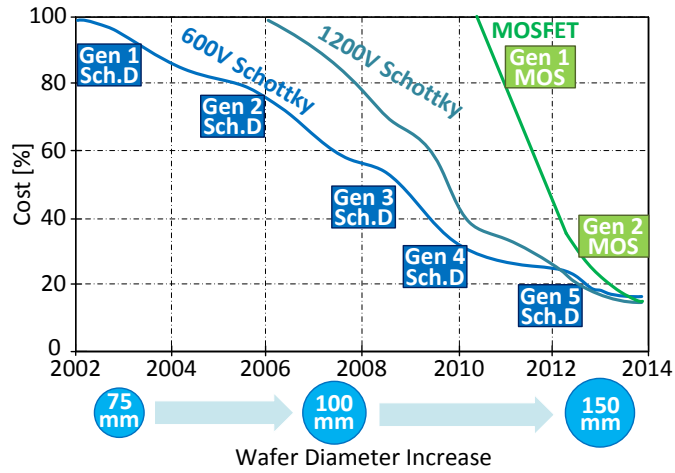


Figure 1-4 Cost reduction curves on a normalized basis of the SiC power device industry [12]

Since then CREE has already released the second generation with a price lower than the first one. There are available on the market with a breakdown voltage from 1.2 kV to 1.7 kV and current ratings from 4 A to 300 A. At this point SiC is the best choice for WBG-power electronic devices due to its relatively mature technology.

The appearance on the market of SiC-based JFET and MOSFET (with power ratings comparable with Si-based devices) has triggered the starting point of a transition stage from Si to SiC-based devices in some applications. The transition phase is strongly influenced by the evolution of the new devices in terms of power ratings, price reduction and device reliability. Nowadays, there is a wide range of SiC-devices available on the market, from discrete to module devices. Table 1-2 presents a comparison between Si and SiC devices which have the same power ratings in terms of: junction to case thermal impedance, threshold voltage, switching losses and costs. It can be seen that the costs of SiC device is around 2-3 times higher and the switching losses are around 6-8 times lower when comparing with the Si-based ones. Moreover, the junction to case thermal impedance and threshold voltage are lower in the SiC case. All these advantages have a positive impact on the power density and switching frequency operation of SiC-devices.

Table 1-2 Commercial Si and SiC devices for 1200 V Publication 7

Device type/ ratings for Tj=100°C	Discrete Devices 1200V, 20A				One-Leg Module 1200V, 100A				Three-Phase Module 1200V, 50A			
Si-IGBT	IHW20T120-Infineon				FF100R12YT3-Infineon				FS50R12KT4B-Infineon			
SiC-MOSFET	C2M0080120D-CREE				CAS100H12AM-CREE				CCS050M12CM-CREE			
Rth(jc) [K/W] Transistor.-F.Diode	Si		SiC		Si		SiC		Si		SiC	
	0.85	1.3	0.6	0.6	0.28	0.48	0.19	0.37	0.54	0.81	0.37	0.42
Threshold Voltage	5.8V		3V		5.8V		2.4V		5.8V		2.3V	
Device Cost Euro Euro/A SiC/Si	5.7		13.5		110		374		138		372	
	0.29		0.67		0.55		1.87		0.46		1.24	
	2.3X				3.4X				2.7X			
Sw. test conditions	800V, 20A, Tj=150°C				600V, 100A, Tj=125°C				600V, 50A, Tj=150°C			
Gate resistance [Ω]	35		6.8		6.8		5		15		20	
Switching loss	Si		SiC		Si		SiC		Si		SiC	
Turn-on Eon [mJ]	2		0.28		9.5		2		5.8		1.1	
Turn-off Eoff [mJ]	1.8		0.27		9		1.4		4.5		0.6	
Revers rec. Err [mJ]	included				6		0.4		3.6		-	

The integration on the actual commercial market [2] of the SiC-devices is emphasized with red dotted line in Figure 1-5. According to their rated power (available on the market today), the main applications that can be covered by this field are PV-inverters, adjustable speed drives, pumps and automotive. Moreover, PV-inverter companies already started to produce converters based on these devices (ex: 20 kW inverters build by SMA with Sunny Tripower 20000TLHE-10 and REFUsol with 020K-SCI) [14][15].

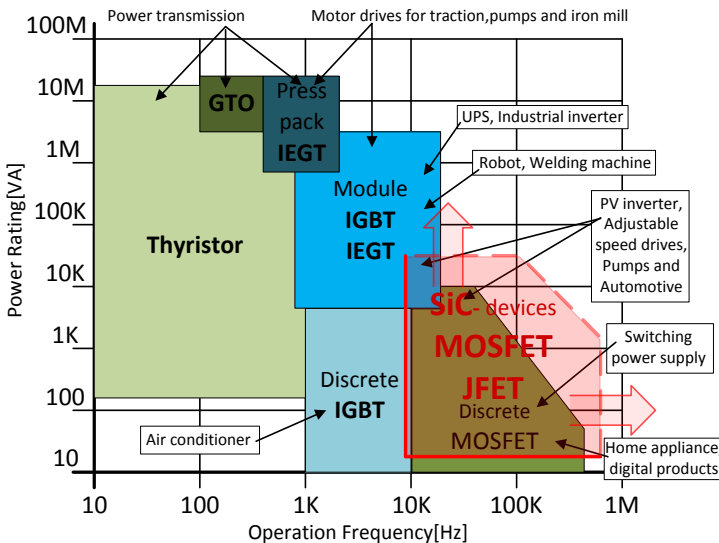


Figure 1-5 The integration on the market of SiC power devices.

Even though SiC-devices have superior electro-thermal properties when compared to Si-based devices, this doesn't mean that they are more reliable. Moreover, there are some studies which claim that if Si and SiC-devices are using the same type of packaging, the reliability of the SiC devices is lower. Therefore, all of this rises the reliability uncertainties of using SiC-devices in nowadays applications. [16-17]

1.4 Emerging challenges of a design tool for reliability

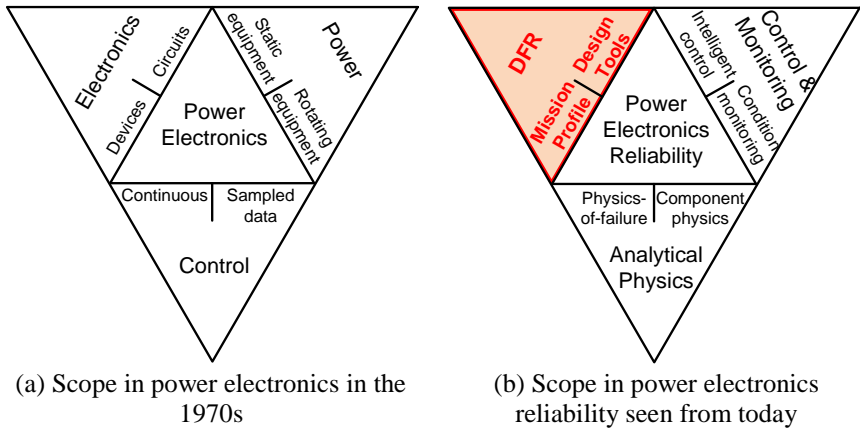


Figure 1-6 Defined scope in: (a) power electronics by William E. Newell in the 1970s [18] and (b) power electronic reliability research seen from today by the Center of Reliable Power Electronics (CORPE) [19].

In 1970s, William E. Newell was the first who defined the scope and concept of “Power Electronics” as combining three of the main disciplines of electrical engineering according to Figure 1-6 (a) [18].

Nowadays, the reliability research in power electronics has a multidisciplinary approach as shown to [19] (Figure 1-6 (b)), covering the following three main aspects:

- Analytical physics analysis to understand the root cause of why and how the power electronics products fail.
- Intelligent control and condition monitoring of the power electronics product, to ensure reliable field operation under specific mission profiles.
- Design For Reliability (DFR) suppose a tool to consider the real

field mission profile operating conditions to achieve the required reliability and robustness of power electronic products.

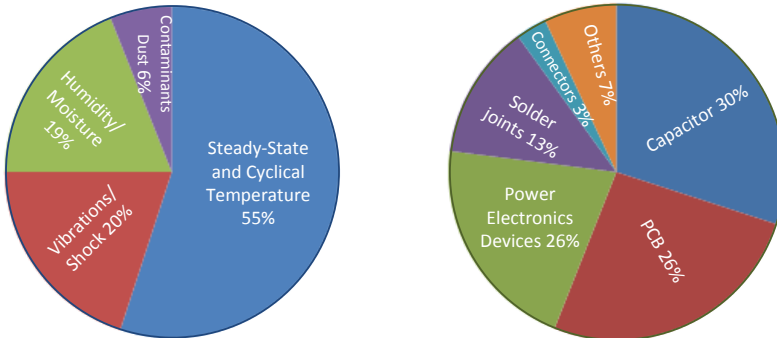
As emphasized with red line in Figure 1-6 (b), a DFR-tool plays a key role into nowadays power-electronics reliability.

Many tools are expected to be developed into this direction by considering the main stressors shown to Figure 1-7 (a). It is worth to mention that temperature is the most important stressor parameter. Therefore, the project will focus the research on developing a tool dedicated for this stressor.

1.4.1 Mission Profile importance in reliability

The converter availability is the most important aspect in renewable energy system applications and it depends on the component and system reliability as well as its maintenance [20, 21]. The field experiences in renewables reveal that power converters are responsible for more than one-third (37 %) of the unscheduled maintenance, and more than a half (59 %) of the associated cost during five years of operation of a 3.5 MW PV-plant [22].

Therefore, highly reliable components are required in order to minimize the downtime during the lifetime of the converter and implicitly the maintenance costs [22-24]. The design of high reliable converters under constrained reliability and cost is a great challenge to be overcome in the future. Figure 1-7 (a) [25] shows the main source of stressors distribution which involves failure in converters, where the temperature is seen to be the most important stressor-parameter.



(a) Source of stress distribution [25]

(b) Failure cause distribution [26]

Figure 1-7 Stress causes (a) and failure distribution (b) in power electronics systems

Due to this cause the failure rate sharing of the main components used in the power converter design has the distribution according to Figure 1-7 (b) [26]. It is worth to mention that semiconductor devices, capacitors and PCBs are the most prone to failure within the converter components [27-29].

The knowledge gained from the field data and simulations of high power devices concluded that for each 10°C increase in device temperature the failure rate is almost doubled. Therefore, the temperature variation of the semiconductor devices plays a key role in the robustness design and reliability of power electronics converters. This factor has a major impact on the power converters used in renewable energy systems, like solar and wind energy applications, due to the fluctuating nature of the mission profile.

Mission Profile (MP) is a representation of the relevant environmental conditions, which have a direct impact in device junction temperature thus in the device lifetime, (through the full life-cycle to the end of life) and they can be represented by: ambient temperature, solar irradiance (for PV-inverters) and wind speed (for wind-turbine converters). Long term mission profile variations introduce converter current changes which further cause device junction temperature variations (due to the power loss dissipation) that significantly reduce the reliability of the semiconductor devices [30].

The loading stress (e.g. thermal loading of devices, cyclic load, voltage etc.) of the converter devices is a consequence of the MP variations. Moreover, the device strength model is a consequence of the many resisting physical properties (e.g. hardness, melting point, adhesion, etc.) which defines how much loading the component can withstand [21]. A component failure occurs when the applied stress exceeds the designed strength. By analyzing the overlap area between the stress distribution and the strength distribution (Figure 1-8), the probability of failure can be obtained. Therefore, stress and strength, are two of the most important factors which have to be considered for lifetime or reliability estimation of converters.

Moreover, the MP variation from one region to another may change the operating conditions (e.g. from MP1 soft-environment to MP2 harsh-environment) and it will have an impact in the device degradation (e.g. D1 and D2) involving different failure distribution as shown in Figure 1-8.

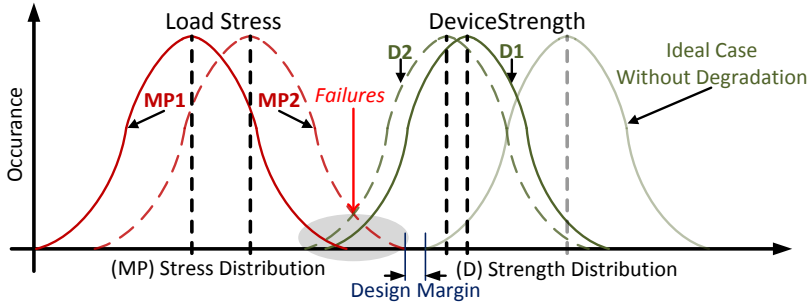


Figure 1-8 Stress-Strength analysis emphasize the overstress failure due to mission profile variation and device aging

The device strength is usually well known, thus the main factor which influence the failure distribution is the MP, which usually is not taken into consideration by the producers in the design stage of the converters. If the stress has the distribution according to Figure 1-8, the converter has a lower lifetime if it is operating under MP2 (which involves D2) when compared with MP1 (which involves D1). This is one of the reasons why converter lifetime in renewable energy applications may vary in a large range. Large variations of the converters lifetime are encountered due to the MP variation from one region to another. Therefore, in order to achieve reliability improvement and cost reduction of the renewable energy technology, it is of major importance to have a lifetime prediction of the converter, according to the real field MP operating conditions.

1.4.2 Translation of the long-term Mission-Profile to device-level thermal loading

It is very important to consider the MP of the field where the converter is operating in the reliability studies in order to better optimize the converter design margin selection (avoid overdesign or underdesign of the product) which will have a positive impact in the cost reduction of the renewable energy technology. Therefore, a reliability-oriented design tool is of great interest and it is highly expected to perform the long-term (e.g. one year) electro-thermal and then the reliability aspect analysis of the switching devices in the new generation of power converters.

The translation of the real field mission profile operating conditions to the device level thermal loading is of importance in order to achieve more realistic lifetime estimation. In this context, it is expected to link

the physics of the power device to a large scale system simulation within a reasonable framework of time and accuracy.

Previous studies of lifetime prediction focus either at device level [31, 32], which assume constant temperature cycling during operation, or at system level [33-39].

In nowadays state-of-the-art, the studies performed at system level [33-39] presents an inaccurate approach of translating the long term MP to the device level thermal loading. The inaccuracy of these models comes due to the following issues:

- The above mentioned studies rely on lookup-tables based electro-thermal models defined in Plects toolbox from Matlab. This model considers the device datasheet values for at least two temperatures in order to define the curve equations and afterwards they apply an interpolation between the curves.
- In Plects toolbox it is not possible to introduce the device junction temperature as a model input and to see the impact on device power losses. In order to build a long term simulation model this information is required. Therefore the data used are not accurate.
- The main fact which introduces the highest error in the above mentioned models is that they are not able to consider the impact of heatsink time response in the junction temperature estimation. These models are performing a long term simulation by considering a constant temperature of the heatsink which is not changing during the operation. Therefore, the estimated device junction temperature is not accurate.
- To improve the accuracy, the electro-thermal model should also consider the device aging influence into the junction and case temperature estimation for a long term operation.
- Beyond the models accuracy, the MP sampling-time variation plays a key role in the lifetime-estimation error. Therefore it is important to understand the impact of this parameter in the lifetime estimation.

In order to achieve a more accurate translation of the long-term MP to the device-level thermal loading, the mentioned challenges should be solved.

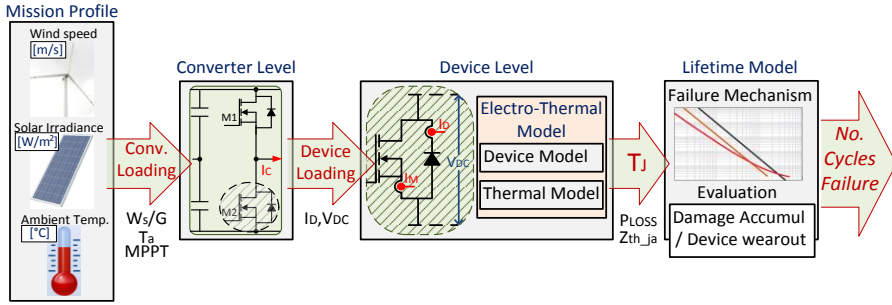


Figure 1-9 Design tool for reliability studies approach-flow

Figure 1-8 presents the required steps in translating the MP down to device level loading, than to device junction temperature T_j estimation and finally to the expected device lifetime. Moreover the main parameters which are involved in each translation stage could also be seen.

Depending on the applied loading profiles, the information for reliability design can be used to optimize the design and selection of power modules for particular applications. Moreover, by estimating the lifetime with a known accuracy and confidence bounds, the system reliability can be improved by replacing the devices before their failure.

Besides this, another important method for improving the reliability can be obtained by active thermal control of the devices. Nowadays, there are some studies into this direction, which mainly focus on control methods for improving the reliability through the device power loss variation by the switching frequency variation or by circulating the reactive power [40-43].

These methods are not so efficient because they cannot achieve an accurate thermal control in a wide range of loading variations. Therefore this tool can be used to assess the impact in device lifetime when implementing various thermal control strategies.

The design tool is of great interest for the new generation of power converters, which are based on SiC-devices, due to their superior electro-thermal properties which involves a higher temperature operating point compared to the Si-based devices [16, 44].

Therefore, in order to achieve reliability improvement and cost reduction of the renewable energy technology, it is of major importance to have the lifetime prediction of the converter, according to the MP variation operating conditions which may lead to:

- A better converter design margin selection in order to avoid overdesign or underdesign of the product.
- The information for reliability design can be provided to optimize the design and selection of power modules for particular applications.
- By estimating the lifetime with a known accuracy and confidence bounds, the system reliability can be greatly improved by replacing the devices before their failure.
- Assess the impact on power electronics device lifetime when applying various thermal control strategies.

1.5 Project objectives

The integration of SiC devices into a market dominated by Si is strongly influenced by their evolution in terms of power ratings, price reduction and also device reliability.

Therefore, in order to achieve reliability improvement and cost reduction of the new generation of power converters used in renewable energy systems, the emerging challenges that need to be overcome are summarized as follows:

1. How can the translation of the real field mission-profile operating conditions to the device level thermal loading be achieved within a reasonable framework of simulation time and accuracy?
2. What is the impact of the long term mission-profile variation (e.g. one year), gate-driver parameter variation and mission-profile sampling-time variation in the lifetime-estimation accuracy?
3. Can any reliability improvement of the SiC-devices be achieved by using a novel active-thermal control method?

Based on the above mentioned research problems, the main objective of the PhD project are:

1. Develop a Reliability-Oriented Design tool for the new generation of power converters used in renewable energy systems.

2. Develop a method for enhancing the lifetime of power semiconductor devices which relies on an Advanced Gate-Driving concept.

As a study case, this thesis focuses on the inverters used in PV-system applications.

1.6 Thesis outline

The thesis is presented as a collection of papers and is divided into two main parts: Part I – REPORT and Part II – PUBLICATIONS. Part I summarizes the research work that has been carried out during the PhD study to answer the research questions, structured in five chapters and Part II lists all the selected publications that have been presented in international conferences and in journals.

Chapter 1 – Introduction – gives the background and motivation of this research. Moreover, it investigates the state-of-the-art SiC-power electronic devices technology and introduces what are the emerging challenges of a design tool for reliability which is based on a real field mission profile. Finally the main objectives and outline of the thesis are listed.

Chapter 2 – Mission-Profile Reliability-Oriented Design Tool – introduces a novel concept of assessing the reliability of power semiconductor devices by considering the device degradation and the mission profile operating conditions. The detailed modeling process of the tool is presented consisting of: Real Field Mission Profile model (for soft and harsh environment operating conditions), a grid connected PV-inverter model, an Electro-Thermal model, and a Lifetime model. Afterwards the translation process from the Detailed Simulation Model to the Long Term Simulation Model in order to consider the mission profile impact on device thermal loading is presented.

Chapter 3 – Model Validation and Lifetime Analyses of SiC-based PV-inverter Devices – this chapter presents the electro-thermal model validation and the reliability studies performed by the proposed tool. The validation of the proposed electro-thermal model is done for device level and for system level operation. As a study case is proposed and implemented a SiC-based PV-inverter cost competitive with a Si-based

one, by taking the advantage of the main opportunities offered by these devices. The chapter ends with a detailed lifetime analysis, which emphasizes the mission-profile variation and gate-driver parameters variation impact in the proposed PV-inverter devices lifetime. Moreover, the impact of mission-profile sampling time on the lifetime estimation accuracy is also determined.

Chapter 4 – A Novel GD-Concept for Enhancing the Reliability of Power-Semiconductor Devices – presents a novel gate-driver concept which reduces the dependency of the device power losses variations on the device loading variations. The proposed gate-driver is able dynamically and accurately to control the gate-resistance and gate-voltage in order to preserve constant the device losses dissipation, implicitly also the device temperature. The impact of the novel gate driver concept in the active thermal control of the power electronics devices is presented. In order to proof the concept, the hardware implementation of the proposed active thermal control has been done. Furthermore, a novel gate-driver strategy for improvement of the power devices reliability is proposed. The chapter ends with a detailed lifetime analysis, which emphasizes the mission profile variation and advanced gate-driver strategy impact on the converter device lifetime.

Chapter 5 – Conclusions and Future Work – concludes the research done in the thesis, summarizes the main contributions and discuss some potential proposals for future work.

PART II of the thesis is entitled PUBLICATIONS and presents the complete list of articles-papers published in international conference proceedings and journals that were achieved based on the obtained results during this research period.

1.7 List of publications

The work performed during the PhD studies has been presented in eight publications, three journal-papers and five conference-papers as follows:

Journal papers:

- P. I.** **C. Sintamarean**, F. Blaabjerg, H. Wang and Y. Yang, "Real Field Mission Profile Oriented Design of a SiC-Based PV-Inverter application", IEEE Transactions on Industry Applications, Vol. 50, no. 6, pp. 4082-4089, 2014.
- P. II.** **C. Sintamarean**, F. Blaabjerg, H. Wang and P. De P. Rimmen, "A design tool to study the impact of mission-profile on the reliability of SiC-based PV-inverter devices", ESREF-Microelectronics Reliability, pp. 1655-1660, 2014.
- P. III.** **C. Sintamarean**, F. Blaabjerg, H. Wang F. Iannuzzo and P. De P. Rimmen, "Reliability Oriented Design Tool for the New Generation of Grid Connected PV-Inverters", IEEE Transactions on Power Electronics-Special Issue in Reliability, Vol. 30, no. 5, pp. 2635-2644, 2015.

Conference papers:

- P. IV.** **C. Sintamarean**, F. Blaabjerg, and H. Wang, "A Novel Electro-Thermal Model for Wide Bandgap WBG-semiconductor based devices", IEEE European Conference on Power Electronics and Applications (EPE –ECCE Europe), pp. 1-10, 2013.
- P. V.** **C. Sintamarean**, F. Blaabjerg, and H. Wang, "Comprehensive Evaluation on Efficiency and Thermal Loading of Associated Si and SiC based PV Inverter Applications", IEEE Industrial Electronics Society (IECON) , pp. 555-560, 2013.
- P. VI.** **C. Sintamarean**, F. Blaabjerg, H. Wang and Y. Yang, "Real Field Mission Profile Oriented Design of a SiC-Based PV-Inverter application", IEEE Energy Conversion Congress and Exposition (ECCE), pp. 940-947, 2013.
- P. VII.** **C. Sintamarean**, E. Eni, F. Blaabjerg, R. Teodorescu, and H. Wang, "Wide-band gap devices in PV systems-opportunities and challenges", IEEE International Power Electronics Conference

(IPEC-ECCE Asia), pp. 1912-1919, 2014.

- P.VIII. C. Sintamarean**, F. Blaabjerg, H. Wang and F. Iannuzzo, “The Impact of Gate-Driver Parameters Variation and Device Degradation in the PV-Inverter Lifetime”, IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2257-2264, 2014.

Chapter 2

Mission-Profile Reliability-Oriented Design Tool

This chapter presents the modeling process of the proposed reliability oriented design tool. The chapter is divided into five main sections. In the first four sections is presented the detailed modeling process of the tool, starting with the modeling of mission profile and PV-inverter, continuing with the device electro-thermal modeling and ending with the device lifetime model. The last section presents the proposed long term simulation model in order to perform a PV-inverter lifetime analysis considering a one year MP for soft and harsh operating conditions.

The first version of the tool, presented in P. I and P. VI, has not included into the model the impact of heatsink time response. Due to this issue, this tool could be applied only for the following study cases:

- Applications which are using discrete devices which require a heatsink with a time response lower than the mission-profile sampling time.
- Applications which are using liquid-based cooling system but they are always operating at the same cooling temperature for the device base-plate.

In order to overpass these issues, an improved and final version of the tool has been proposed in P. II and P. III.

The translation of the real field mission profile PV-inverter operating conditions to the device level thermal loading is of great interest. In order to achieve a realistic lifetime estimation, it is expected to link the physics of the power devices into a large scale system simulation within a reasonable framework of time and accuracy.

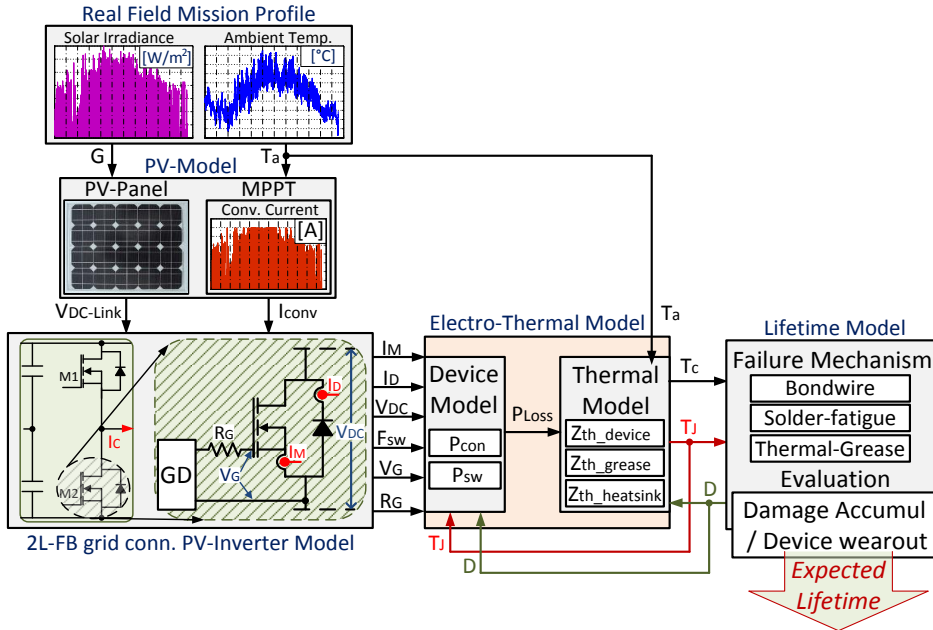


Figure 2-1 Proposed reliability oriented design structure for a new generation of grid connected PV-inverters.

In this context, this project introduces a reliability oriented design tool for a new generation of grid connected PV-inverters.

According to Figure 2-1, the proposed design tool consists of a Real Field Mission Profile (RFMP) model, a PV-panel model, a grid connected PV-inverter model, an electro-thermal model and a lifetime model. The proposed model considers also the impact of the gate-driver parameters and device degradation in the lifetime estimation.

The involved parameters emphasized in Figure 2-1 are as follows: G - solar irradiance, T_a - ambient temperature, $V_{DC-Link}$ - DC-Link voltage, I_{conv} - converter output current, I_M - MOSFET drain current, I_D - freewheeling diode current, V_{DC} - device off-state voltage, F_{sw} - switching frequency of the device, V_G - gate voltage, R_G - gate resistance, $Z_{th_device/grease/heatsink}$ - junction to case/grease/heatsink thermal impedance, T_J - device junction temperature, T_c - case temperature of the device, D - device degradation (aging).

Furthermore, in order to have a better understanding of the proposed reliability oriented design tool, a detailed description of each part is presented below.

2.1 Real Field Mission Profile model

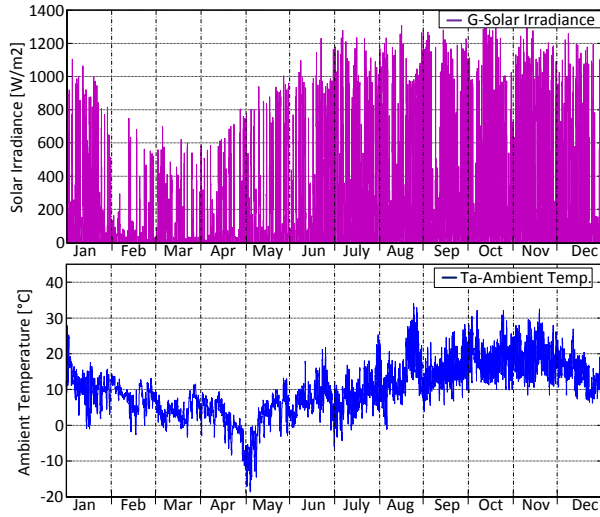


Figure 2-2 The Real Field Mission Profile (RFMP) data for one year measurements of solar irradiance G and ambient temperature T_a in soft environmental operating conditions (Aalborg-Denmark).

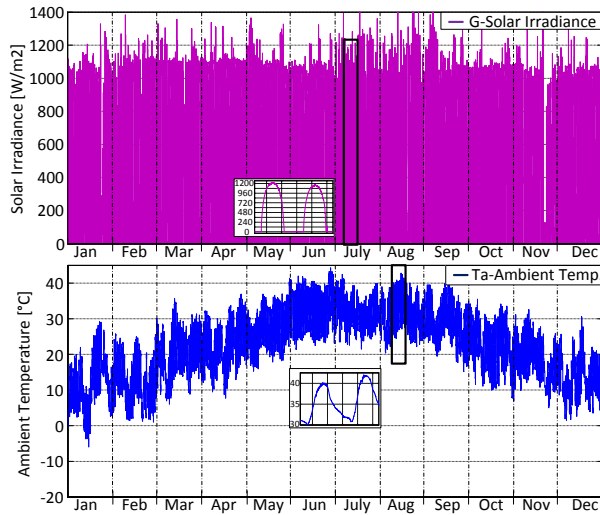


Figure 2-3 The Real Field Mission Profile (RFMP) data for one year measurements of solar irradiance G and ambient temperature T_a in harsh environmental operating conditions (Arizona-USA).

The proposed design tool presented in Figure 2-1 considers the mission profile (MP) of the real field, where the converter will operate. The mission profile is a representation of the relevant environmental

conditions, which has a direct impact on device junction temperature and thus in the device lifetime, (through the full life-cycle to the end of life). For PV-inverters the MP is represented by ambient temperature and solar irradiance.

The mission profile model is developed based on one year measurements of solar irradiance (G) and ambient temperature (T_a) for two different locations. In order to study the MP-variation impact on the PV-inverter devices reliability, harsh and soft environmental conditions are selected from two different locations: the first one (soft environment conditions) is from Aalborg-Denmark (Figure 2-2) and the second one (harsh environment) from Arizona-USA (Figure 2-3). The MPs were selected from a set of ten locations around the world. The data were provided by Danfoss Solar but the developed tool can use any mission profile. In order to select the softest-harshesht environmental operating conditions, the rain-flow counting algorithm has been used. The sampling time of the measured data is one minute. Thus a realistic loading of the converter devices can be achieved.

2.2 Grid-Connected PV-inverter Model

It can be clearly seen in Figure 2-1 that the device current and the off-state voltage are required in the electro-thermal model. In this purpose the inverter model is developed in order to estimate the current flow through the device, and the off-state blocking voltage of the device according to the operating conditions.

A typical grid connected PV-system is shown in Figure 2-4 and it consists of: the voltage source inverter (VSI), the output LCL-filter and the PV-strings.

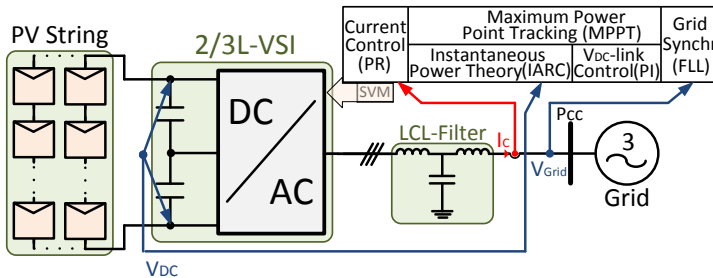


Figure 2-4 Grid-Connected PV-inverter

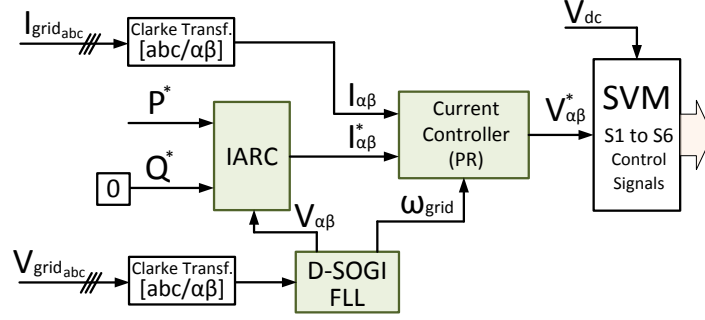


Figure 2-5 Control strategy structure

The use of a boost-converter stage (between the PV-strings and inverter) is optional and depends mainly on the PV-system power. Moreover, Figure 2-4 presents also the main control blocks to achieve the PV-system functionalities.

The overall system simulation (control and model of the converter) has been performed by using Matlab/Simulink and the PLECS toolbox. The main control architecture is presented in Figure 2-5 and the system is using as input signals: the grid current (I_{grid_abc}) for loop feedback and the grid voltage (V_{grid_abc}) for synchronization.

In order to achieve the desired system functionalities a resonant current controller for fundamental frequency is used. The complexity of the stationary reference frame current control implementation is lower than in the dq control structure, as dq transformations, cross-coupling terms and feedforward voltages are not needed. Hence, an accurate current control may be achieved, as the current controller poles will be placed to provide infinite gain for 50 Hz. [45]

The synchronization method used in this control strategy is based on a double Second Order Generalized Integrator Frequency Locked Loop (DSOGI-FLL) algorithm.[46] As a result, the fundamental frequency is continuously estimated for online tuning of the resonant controllers.

In order to provide or absorb a desired quantity of active or reactive power into the grid by using a power converter, special attention has to be given to the Instantaneous Active and Reactive power Control (IARC) which has been implemented according to [47].

In simulation, the control has been implemented in C-code by using S-Function Builder blocks from Matlab/Simulink in order to achieve a more realistic approach to a real system behavior. Therefore, it is

necessary to design the current controller for a discrete time system.

In the stationary reference frame, high performances are achieved by designing a controller with a complex pole, a very low damping factor and a characteristic frequency equal to the desired one (ω_g).

In this case the discrete resonant controller transfer function has been obtained considering [48] and it has the following form (2.1):

$$C[z] = K \frac{z^2 + \alpha_1 z + \alpha_2}{z^2 - 2\cos(\omega_g \Delta t)z + 1} = 2.31 \frac{z^2 - 1.782z + 0.891}{z^2 - 1.895z + 1} \quad (2.1)$$

Where K and the zeros of the controller transfer function are the design parameters, and Δt is the sampling period. By taking into consideration the controller transfer function and the discrete transfer function of the filter it is possible to obtain the final model, as it is shown in Figure 2-6. Furthermore, a unit sample delay has been introduced in order to represent the sampling and the calculation time of the processor.

The design parameters have been obtained by introducing the current control design loop into MATLAB/SISO-Tool graphical interface.

As a study case is considered a grid-connected 2L-FB PV-inverter application which has the parameters presented in Chapter 3. The obtained results for the 50 Hz current controller are given in (2.1).

The root-locus and the closed loop bode diagram presented in Figure 2-7 (a), shows that the system is stable and that the controller is selective for the grid frequency of 50 Hz. When a step in active power from 0 to the rated converter power (25 kW) is provided as a reference, according to Figure 2-7 (b) the converter is injecting the rated peak current (alpha axis) to the grid (52 A). The proposed process flow from this section is further considered in the thesis for the studies which involves PV-inverter applications.

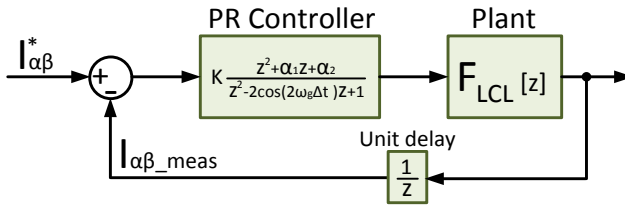


Figure 2-6 Current control design loop

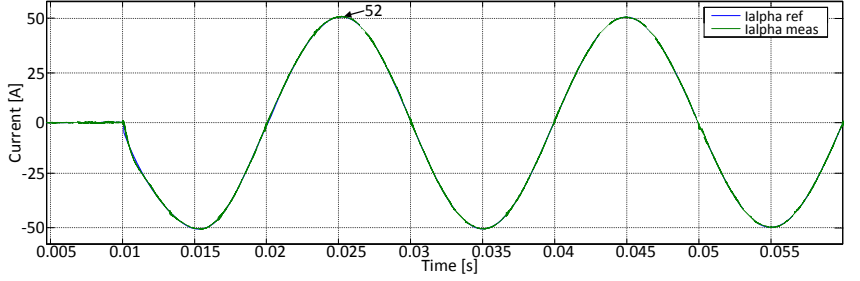
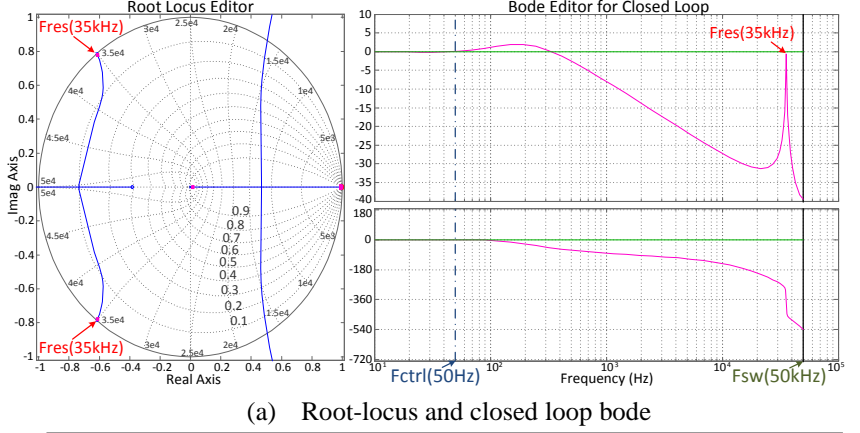


Figure 2-7 (a) Root-locus and closed loop bode response for 50 Hz current control design parameters and (b) alpha axis current response reference and measured

2.3 Electro-Thermal Model

The proposed model aims at estimating the junction and case temperature for the new generation of power electronics devices by considering also the impact of aging and gate-driving conditions. A detailed description of the model has been presented in Publication 4.

The input signals in the model are: the realistic device (MOSFET and Diode) loading current (I_M or I_D) and voltage variations (off-state voltage V_{DC}), the switching frequency (f_{SW}), the ambient temperature (T_a), the gate-driver operation point (V_G and R_G) and the device degradation level (D). Figure 2-8 presents the proposed electro-thermal model where three types of models are involved: the device model and the thermal model which are linked together by the power loss model.

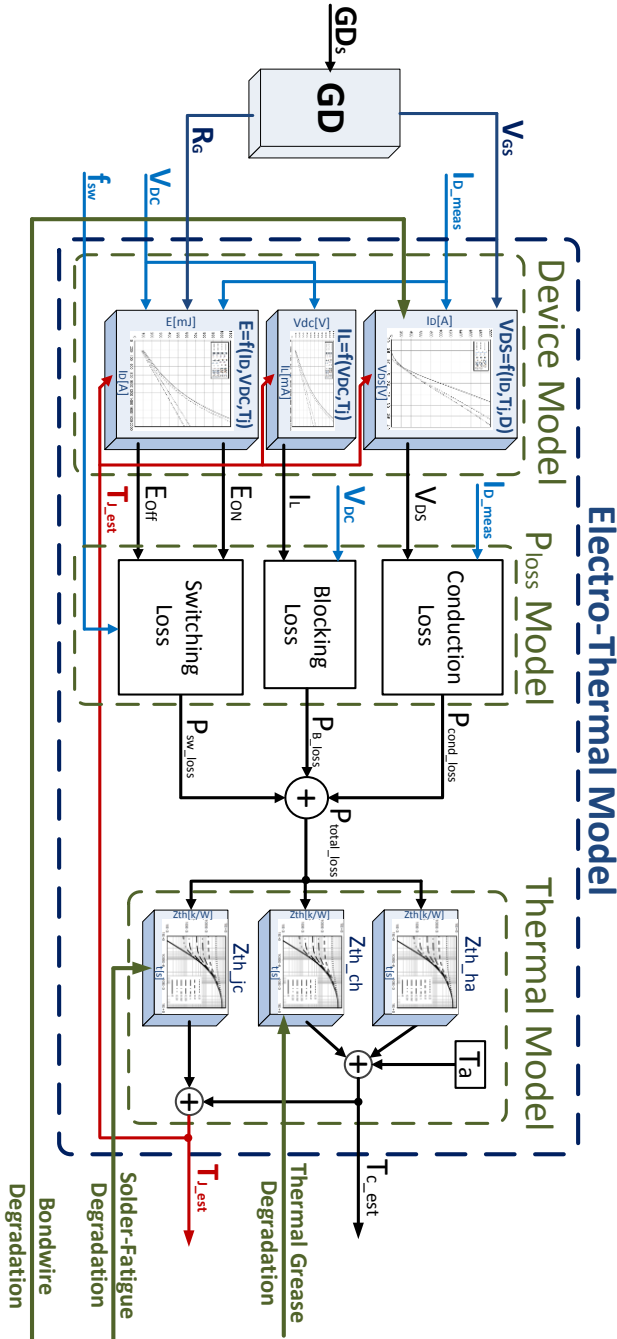


Figure 2-8 Proposed Electro-Thermal model structure for device junction and case temperature estimation

In the first instance, the device model is responsible of estimating the device on-state voltage drop (V_{DS}) and switching energies (E_{ON} and E_{Off}) by considering the current (I_D), the off-state blocking voltage (V_{DC}), the junction temperature (T_J) and the device degradation-aging (D).

The above mentioned parameters and the switching frequency are further used and included into the power loss P_{Loss} model, where the instantaneous conduction and switching losses of the device are determined. Furthermore, the thermal model estimates the device junction and case temperature by considering the total power loss and ambient temperature. It is worth to mention that the thermal model consists of the device junction to case thermal impedance ($Z_{th_{jc}}$), thermal grease thermal impedance ($Z_{th_{ch}}$) and heatsink thermal impedance ($Z_{th_{ha}}$). Finally, by providing as a feedback the estimated junction temperature into the device model, the temperature impact into the losses is also included.

Moreover, the electro-thermal model considers the device degradation, the thermal degradation and gate driving parameters influence into the junction and case temperature estimation as follows:

- Device aging - in terms of on-state resistance degradation R_{on} (due to bondwire lift-off).
- Thermal aging - in terms of junction to case thermal impedance degradation $Z_{th_{jc}}$ (due to solder fatigue) and case to heatsink thermal impedance degradation $Z_{th_{ch}}$ (due to thermal grease wear-out).
- Gate-driving parameters impact in terms of gate voltage V_G and gate resistance R_G .

2.3.1 Device model

The device model estimates the on-state voltage drop and switching energies by considering the current, the off-state blocking voltage, the junction temperature and the device degradation-aging.

Furthermore, the estimated parameters and the switching frequency will be used into the loss model (P_{Loss}) where, the instantaneous conduction (P_C), blocking/leakage (P_B) and switching losses (P_{SW}) of the device are calculated. Moreover, the total losses ($P_{tot_{loss}}$) and the ambient temperature (T_a) are fed into the thermal model which estimates the device case (T_c) and the junction temperature (T_J). Finally, by providing

the junction temperature as a feedback to the device model, the temperature impact is considered.

The total losses ($P_{\text{tot_loss}}$) of the device are given by:

$$P_{\text{tot_loss}} = P_C + P_{SW} + P_B \quad (2.2)$$

2.3.1.1 Conduction losses estimation model

The device (MOSFET, diode) conduction losses are produced by the product of the on-state voltage drop (drain-source voltage V_{DS} , forward voltage V_F) across the power device and the instantaneous value of the current (MOS current I_D , diode current I_F) which is flowing through it. As shown in Figure 2-10, they occur during the device conduction time (T_{on} on-state time) and they can be calculated as:

$$P_C(t) = \frac{1}{T_{\text{on}}} \int_{T_{\text{off}}}^{T_{\text{off}}+T_{\text{on}}} v_{DS}(t) \cdot i_D(t) dt \quad (2.3)$$

Assuming that the device current (I_D , I_F) is known, to achieve an accurate calculation of the conduction losses the on-state voltage (V_{DS} , V_F) has to be estimated. Therefore a model, which estimates the device on-state voltage by considering the device current and junction temperature variations is needed.

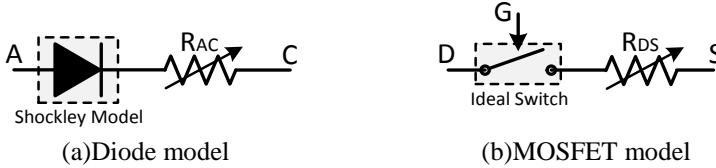


Figure 2-9 Proposed Shockley-based diode model (a) and MOSFET model (b) by considering also the internal resistance variation

Diode on-state voltage estimation:

An accurate estimation of the diode forward voltage drop (V_F) can be achieved by combining the Shockley model [49] with the resistance model (Figure 2-9 a). Therefore, the used equation which uses this estimation has the following form:

$$V_F = n \cdot V_{Th} \cdot \ln\left(\frac{I_F}{I_S} + 1\right) + R_{AC} \cdot I_F \quad (2.4)$$

Where: V_F – on-state voltage, n – a correction constant which has been determined in order to improve the estimation accuracy of the on-state voltage, V_{Th} – device thermal voltage, I_F – device current, I_S – the saturation current, R_{AC} – device on-state resistance.

The above mentioned parameters are modeled as a function of the junction temperature T_J variation. The V_{Th} estimation is done according

to (2.5) (considering the T_J into the studies) where $k=1.38 \cdot 10^{-23}$ J/K is the Boltzmann constant and $q=1.60 \cdot 10^{-19}$ J/V is the elementary electron charge.

$$V_{Th} = \frac{k \cdot T_J}{q} \quad (2.5)$$

Moreover, the impact of T_J in the saturation current I_S is determined as follows:

$$I_S = \alpha \cdot e^{\frac{T_J - T_{ref}}{\beta}} \quad (2.6)$$

Where α and β coefficients are determined by a least square curve fitting method, which considers the values available from the laboratory measurements for different temperatures. Finally, the on-state resistivity variation according to the temperature is obtained in (2.7) as:

$$R_{AC} = [a \cdot (T_J - T_{ref}) + 1] \cdot R_0 \quad (2.7)$$

Where: a – is the temperature coefficient, T_{ref} – the reference temperature for which temperature coefficient is mentioned, R_0 – is the initial on-state resistance at temperature T_{ref} .

MOSFET on-state resistance estimation:

As shown in Figure 2-9 (b) the MOSFET is modeled as an ideal switch in series with a resistance. In order to include the temperature impact on the on-state drain-source resistance (R_{DS}), equation (2.7) is used. Therefore, the MOSFET on-state voltage drop (V_{DS}) estimation is performed as:

$$V_{DS} = I_D \cdot [a \cdot (T_J - T_{ref}) + 1] \cdot R_0 \quad (2.8)$$

Finally, Table 2-1 presents the obtained parameters values for the mentioned SiC-devices.

Table 2-1 MOSFET and diode model parameters

SiC Devices CREE	Estimated Parameters	
Diode C4D20120A	On-state resistance [Ω]	$R_{AC} = [0.01177 \cdot (T_J - 273.15) + 1] \cdot 0.019$
	Saturation current [A]	$I_S = 0.00042 \cdot e^{\frac{T_J - 273.15}{25.2}}$
	Thermal voltage [V]	$V_{Th} = \frac{1.38 \cdot 10^{-23} \cdot T_J}{1.6 \cdot 10^{-19}}$
MOSFET CMF20120D	On-state resistance [Ω]	$R_{DS} = [0.00407 \cdot (T_J - 273.15) + 1] \cdot 0.07356$

2.3.1.2 Blocking losses estimation

The blocking losses are produced by the off-state blocking voltage V_{DD} and the leakage current I_{LM} of the power device. They occur during the off-state time of the device and they are calculated as:

$$P_B(t) = \frac{1}{T_{off}} \int_{T_{on}}^{T_{on}+T_{off}} v_{DD}(t) \cdot i_L(t) dt \quad (2.9)$$

The off-state voltage and the temperature of the semiconductor chip influence the leakage current. The value of this current is very low, thus these losses can be neglected.

2.3.1.3 Switching losses estimation

MOSFET switching losses estimation:

When the device commutation from ON-state to OFF-state (or opposite) is performed, the voltage and the current are not changed instantaneously. The main consequence of this transient period (Figure 2-10 a) is the switching power losses dissipation. These losses depend on the switching energy losses for turn-on (E_{on}) and turn-off (E_{off}) process as well as the switching frequency, which is shown in equation (2.10).

$$P_{SW} = (E_{on} + E_{off}) \cdot f_{SW} \quad (2.10)$$

As shown in Figure 2-10 (a), these energies depend on the dynamics of the commutation process so they may be difficult to calculate. The estimations of the E_{on} and E_{off} are done by using (2.11) and (2.12).

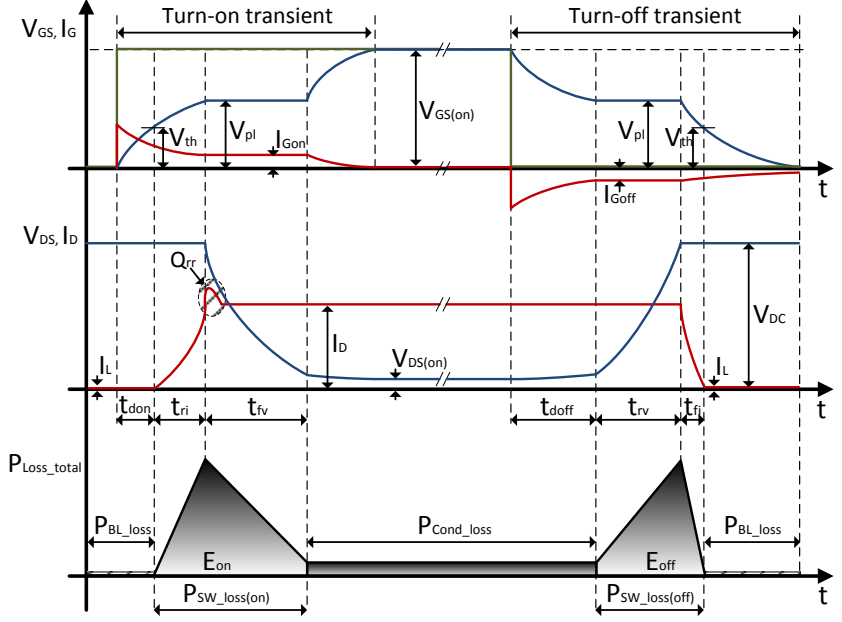
$$E_{on} = \int_0^{t_{ri}+t_{fv}} v_{DS}(t) \cdot i_D(t) dt = E_{onM} + E_{onDrr} = V_{DD} \cdot I_D \frac{t_{ri} + t_{fv}}{2} + Q_{rr} \cdot V_{DD} \quad (2.11)$$

$$E_{off} = \int_0^{t_{rv}+t_{fi}} v_{DS}(t) \cdot i_D(t) dt = V_{DD} \cdot I_D \frac{t_{rv} + t_{fi}}{2} \quad (2.12)$$

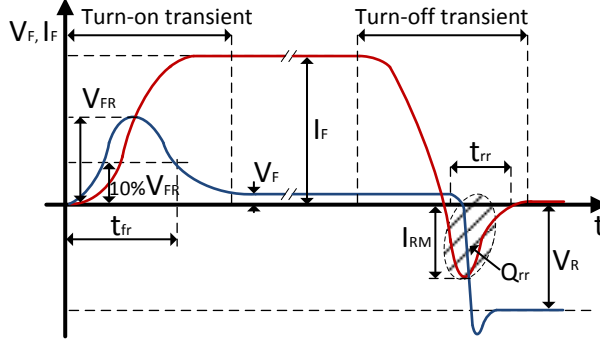
Where: t_{ri} – rise time of the current, t_{fi} –fall time of the current, t_{rv} –rise time of the voltage, t_{fv} –fall time of the voltage, Q_{rr} –reverse recovery charge of the diode, I_D – device current, V_{DD} – device blocking voltage.

The device current I_D and voltage V_{DD} are known thus, the parameters that have to be estimated in order to achieve the calculation of the energies E_{on} and E_{off} are the commutation times t_{ri} , t_{fi} , t_{rv} , t_{fv} and the diode Q_{rr} . The turn-on and turn-off switching times (2.13) are changing according to the off-state blocking voltage, drain current and junction temperature variations.

$$t_{r/f} = f(V_{DD}, I_D, T_J), V_{DD} \in 0 \div 1200V, I_D \in 0 \div 40A, T_J = 25 \text{ and } 150^\circ C \quad (2.13)$$



(a) MOSFET switching transients



(b) Freewheeling Diode switching transients

Figure 2-10 Turn-on and turn-off switching waveforms and energy losses of the device.

Table 2-2 Turn-on and turn-off commutation times

	Current	Voltage
Rise time (t_r)	$t_{ri} = R_G \cdot C_{ISS} \cdot \ln \left(\frac{V_{GSon} - V_{th}}{V_{GSon} - V_{pl}} \right)$	$t_{rv} = \frac{Q_{GD}}{I_{Goff}}$ where $I_{Goff} = \frac{-V_{pl}}{R_G}$
Fall time (t_f)	$t_{fi} = R_G \cdot C_{ISS} \cdot \ln \left(\frac{V_{pl}}{V_{th}} \right)$	$t_{fv} = \frac{Q_{GD}}{I_{Gon}}$ where $I_{Gon} = \frac{V_{GSon} - V_{pl}}{R_G}$

Where: R_G – gate resistance, V_{GS} – gate voltage, V_{th} – threshold voltage, V_{pl} – plateau voltage, I_G –gate current, Q_{GD} –gate-drain charge, C_{ISS} – input capacitance.

Moreover, the commutation times are determined by considering also the gate-drive parameters (R_G – gate resistance, V_G – gate voltage) according to Table 2-2. The gate-drain charge Q_{GD} is calculated according to equation (2.14) as:

$$Q_{GD} = C_{GD}(V_{DD} - V_{DS}) \quad \text{for} \quad C_{GD} = \frac{C_{GD1} + C_{GD2}}{2} \quad (2.14)$$

The non-linearity of C_{GD} has to be considered in order to improve the accuracy of the rise and fall time estimation. The typical dependence of the gate-drain capacitance C_{GD} on the drain-source voltage V_{DS} is provided in the device datasheet. Therefore a two point approximation is used as follows:

- If the MOSFET is on, C_{GD} takes the value according to the on-state voltage drop, $C_{GD1} = C_{GD}(V_{DS})$.
- If the MOSFET is off, C_{GD} takes the value corresponding to the blocking voltage, $C_{GD2} = C_{GD}(V_{DD})$.

According to Table 2-2 the Miller plateau voltage V_{pl} and the threshold voltage V_{th} are two of the main parameters influencing the rise and fall time of the MOSFET current and voltage. Therefore, the estimation of V_{pl} and V_{th} by considering the drain current, gate voltage and the temperature are of great interest. A method which relies on the typical transfer characteristics curves from the datasheet is used according to [50]. In this context, two points from the same temperature curve are selected. Afterwards, their corresponding drain current (I_{D1} and I_{D2}) and gate-source voltage (V_{GS1} and V_{GS2}) are used in (2.15) to calculate the V_{th} and V_{pl} . It is worth to mention that for a different temperature curve, the same procedure has to be applied.

Finally, the proposed method enables the switching losses estimation by considering the following parameter variation: the device current and voltage, gate-driver parameters and junction temperature impact.

Finally, by using the proposed method, the switching losses can be estimated for different current levels, gate-driver parameters by considering also the temperature influence.

$$V_{th} = \frac{V_{GS1} \cdot \sqrt{I_{D2}} - V_{GS2} \cdot \sqrt{I_{D1}}}{\sqrt{I_{D2}} - \sqrt{I_{D1}}} \quad \text{and} \quad V_{pl} = V_{th} + \sqrt{\frac{I_D}{K}} \quad (2.15)$$

$$\text{Where} \quad I_{D1} = K \cdot (V_{GS1} - V_{th})^2 \Rightarrow K = \frac{I_{D1}}{(V_{GS1} - V_{th})^2}$$

Diode switching losses estimation:

A different approach has been considered for the diode switching losses estimation. The minority carriers from the PN-junction (due to the on-state process) are removed before the diode starts to block the reverse voltage. This causes the reverse recovery current, which influences the turn-off losses of the diode and the additional turn-on losses of the MOSFET. When dealing with a body diode, this current will be absorbed by the MOSFET, causing additional turn-on losses.

The diode current rise time is determined by the MOSFET turn-off time (t_{fi}) and the load current, which defines the dI_F/dt .

The device datasheet shows the turn-on overvoltage V_{FR} and the turn-on recovery time t_{fr} according to the dI_F/dt variation. Thus, the V_{FR} and t_{fr} are determined according to dI_F/dt variation. Finally, the turn-on energy (E_{on}) is calculated as:

$$E_{on} = I_F \cdot V_{FR} \cdot t_{fr} \quad (2.16)$$

The diode-current fall-time is determined by the MOSFET turn-on time and the load current, which defines the dI_F/dt calculation.

Moreover, according to dI_F/dt variation the reverse-recovery time t_{rr} and the reverse-recovery peak current I_{RM} are selected from the datasheet. The turn-off energy (E_{off}) is calculated as follows:

$$E_{off} = I_{RM} \cdot V_R \cdot \frac{t_{rr}}{4} \quad (2.17)$$

All the above mentioned parameters may be seen in Figure 2-10 (b) which presents the switching transients of a diode.

The device datasheet provides the typical output characteristics (considering at two junction temperatures 25 °C and 125 °C) for t_{fr} , V_{FR} , t_{rr} and I_{RM} according to dI_F/dt variation. Therefore, the diode switching energy curves can be calculated for two junction temperatures. By performing an interpolation between the curves, it is possible to estimate the energies for different junction temperature levels. Finally, by multiplying the pulse energies with the switching frequency the turn-on and turn-off switching power losses can be calculated.

2.3.2 Thermal model

Due to the lack of informations required to develop the Cauer-model, the Foster-model has been implemented. In order to understand the approach, the study case presents a discrete device from CREE (CMF20120) which has integrated on the same package (TO-247) the

transistor MOSFET and the freewheeling diode. Figure 2-11 (a) shows the physically internal structure of a module-device emphasizing the power dissipation flow from the semiconductor-chip through the main layers down-to the ambient. Moreover it is worth to mention that the transistor and diode power losses follow through different paths from their own junction to the baseplate, where they merge together by connecting to the same case. Afterwards, they flow through the heatsink and dissipate to the ambient. In order to achieve an accurate estimation of the device junction and case temperature, four main aspects have to be considered in the thermal model:

- The device case temperature is a consequence of the total power loss produced by the transistor and diode.
- Due to the thermal coupling between the transistor and diode, the temperature of the transistor chip (respectively diode) varies also due to the diode chip losses (transistor chip losses).
- The thermal impedance of the device, thermal grease and heatsink has to be properly included in the model.
- The impact of the ambient temperature variations need to be considered too.

Where: Z_{th_jc} – is the device junction-case thermal impedance, Z_{th_ch} – is the thermal grease case-heatsink thermal impedance, Z_{th_ha} – is the heatsink-ambient thermal impedance, T_{j_MOS} – MOSFET junction temperature, T_{j_D} – Diode junction temperature, T_c – case temperature.

All those aspects are included in the proposed thermal-model (Figure 2-11 (b)) which presents the flow from device power losses to the junction temperature considering the impact of: transistor-diode thermal coupling, thermal impedance (of the device, thermal grease and heatsink) and ambient temperature.

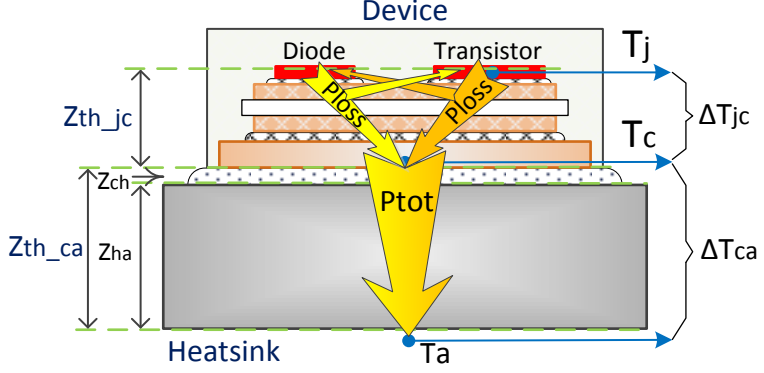
The device thermal impedance is estimated by using a first order transfer functions. The thermal resistance (R_{th}) and time response (τ) parameters are determined by Curve Fitting Tool (CFTOOL) from Matlab according to (2.18).

$$Z_{th_jc} = \sum_{i=1}^n R_i \cdot (1 - e^{\frac{-t}{\tau_i}}) \quad (2.18)$$

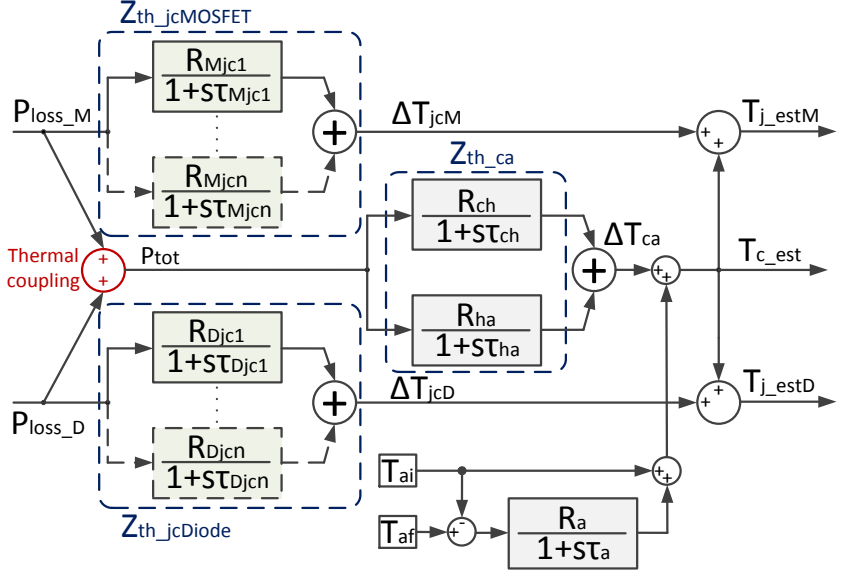
Finally, the estimations of the thermal impedance curves compared to the ones from the datasheets are shown in Figure 2-12 (a) for transistor and Figure 2-12 (b) for diode.

Table 2-3 Device thermal impedance parameter estimation

No.	MOSFET+D-CREE(SiC)			
	MOSFET		Diode	
	$R_{thM}[K/W]$	$\tau_{Mjc}[s]$	$R_{thD}[K/W]$	$\tau_{Djc}[s]$
1.	0.1225	$7.7e-4$	$9.634e-5$	3.692
2.	0.3003	$1.547e-2$	0.01513	3.67
3.	0.5574	37.43	0.2524	$1.536e-3$
4.	0.565	31.05	0.3576	$3.271e-2$

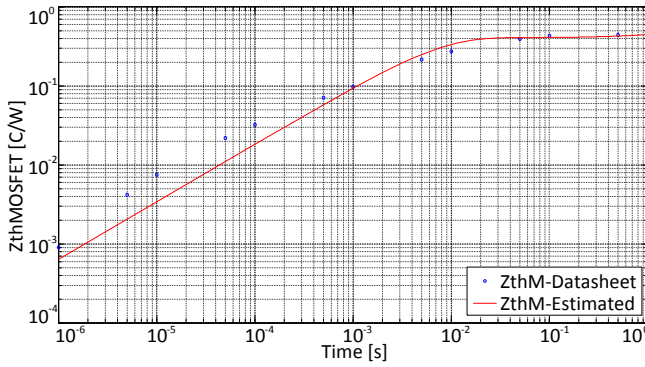


(a)Physically internal structure of the device

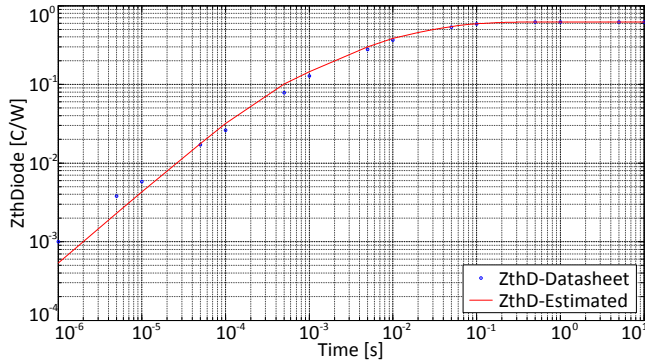


(b)Proposed thermal-model structure

Figure 2-11 Heat dissipation through the internal structure of the device including MOSFET and diode (a) and the proposed thermal model structure (b).



(a) Thermal impedance of the MOSFET



(b) Thermal impedance of the diode

Figure 2-12 Thermal impedance estimation of the device by considering the transistor and its freewheeling diode.

It is worth to mention that for a good estimation of a Cauer-Network a number of four parameters are more than sufficient. The obtained parameters for thermal impedance estimation of the device can be seen in Table 2-3. The thermal impedance and temperature drop across the device and heatsink are shown in Figure 2-11 (a). According to Figure 2-11 it can be seen that by applying the device (MOSFET or diode) loss P_{loss} as input to the estimated thermal impedance Z_{th} , the junction to case temperature drop ΔT_{jc} is obtained. Moreover, by applying the total device power losses (MOSFET + Diode) to the case-to-ambient thermal impedance Z_{th_ca} ($Z_{th_ch} + Z_{th_ha}$) the case-to-ambient temperature ΔT_{ca} is achieved. The ambient temperature variation is also included into the model. Finally, the device case and junction temperatures are obtained by using the following equations:

$$\begin{aligned} T_c &= \Delta T_{ca} + T_a \\ T_j &= \Delta T_{jc} + T_c \end{aligned} \quad (2.19)$$

2.4 Device Lifetime Model

The intensive work on power cycling testing of SiC-power devices is still at the initial stage. Thus at the moment there are not available lifetime models for the analyzed SiC-power module. In order to demonstrate the impact of the proposed reliability tool in the converter design, the state-of-the-art available lifetime models of Si-IGBT modules are considered to be applied for the SiC-devices in the studied case.

In order to achieve a higher level of confidence of the obtained results, the lifetime model of a device with similar power range and packaging is used. Therefore, by having similar packaging, the main difference between the SiC-power device and the Si one is the semiconductor-chip. Due to this approach, the results of the lifetime evaluation could be used for a relative evaluation and comparison studies.

A more relevant lifetime evaluation may be achieved by the replacement with the specific lifetime models of the studied SiC power-modules in the future. Nevertheless, the procedures in the proposed design tool are still valid.

Power electronics devices have various failure models. The reliability of these devices can be studied and analyzed from two main perspectives:

- Semiconductor-chip reliability.
- Device-packaging reliability.

The superior SiC-semiconductor electro-thermal properties when compared to Si, makes the WBG-material to be a good device candidate for high temperature, high frequency operation and high power applications.

One of the main reliability problems, when dealing with the SiC-semiconductor chip has been the gate-oxide break-down.

It has long been a common believe that the gate-oxide grown on SiC-semiconductor is not reliable enough for high temperature operation where SiC-devices are expected to perform [51-54].

Nowadays, based on a literature survey it can be claimed that the thermally-growing of gate-oxide on SiC-semiconductor is intrinsically reliable even at high temperature as 375°C. [55]

Moreover, CREE claims that with the current SiC-processing technology it can be achieved a high reliability of the gate-oxide breakdown, thus for a $V_G=20$ V a lifetime of $1e+07$ hours is achieved [56].

Due to this promising result, it can be stated that the gate-oxide reliability on SiC-material is no longer a problem. Therefore, this project will mainly consider the packaging-related reliability issues into the studies.

The most commonly packaging-related failures are due to the bond-wire damage and the die-attach solder-fatigue [57-58].

The failure mechanisms are mainly triggered by the temperature cycling during operation and the Thermal Expansion Coefficient (CTE) mismatch between the adjacent layers.

There is a correlation between these failures as after die-attach solder is seriously degraded the bond-wire damage is more pronounced [59, 60]. Thus, the solder fatigue will not destroy the device directly, whereas the end of life failure is bond-wire damage related [60]. Therefore, device junction temperature (mean junction temperature T_j and junction temperature variation ΔT_j) is one of the critical parameters required for lifetime estimation.

Based on the previous research works [61] and [62], the failure criteria are defined. Thus, according to [61] an increase of the junction to case thermal resistance $R_{th_{jc}}$ with 40 % indicates a solder-fatigue failure. Moreover, [62] defines the bondwire-damage by the increase of device V_{DS} on-state voltage with 10 %.

Based on the above mentioned literature survey, it can be stated that the device degradation has a linear behaviour for the $R_{th_{jc}}$ while the V_{DS} is mainly changing in the last stage of the lifetime (from 80% to 100%). The degradation impact on $R_{th_{jc}}$ and V_{DS} is presented in Table 2-4.

As shown in Figure 2-8, the proposed electro-thermal model considers the device degradation feedback from the lifetime model. The device degradation is updated according to the consumed lifetime level.

Table 2-4 Device degradation with lifetime level

	Consumed Lifetime level:	Degradation-Aging Impact	
		Normalized $R_{th_{jc}}$	Normalized V_{DS}
1.	0-20%	1	1
2.	20%-40%	1.1	1
3.	40%-60%	1.2	1.01
4.	60%-80%	1.3	1.03
5.	80%-100%	1.4	1.1

As a trade-off between accuracy and simulation time, five degradation levels are included according to Table 2-4. In this way the degradation impact on the device power losses is also included.

Table 2-5 Device lifetime-model parameters [63]

Parameter:	Value:	Unit:	Experimental conditions
Technology factor: A	3.4368e+14	-	Junction temp. variation: $64 \text{ K} \leq \Delta T_J \leq 13 \text{ K}$
α	-4.923	-	
β_0	1.942	-	
β_1	-9.012e-3	-	Bond-wire aspect ratio: $0.19 \leq ar \leq 42$
C	1.434	-	
Υ	-1.208	-	
Diode chip-thickness: d_{Diode}	0.6204	-	Cycling period: $0.07 \text{ s} \leq t_{\text{on}} \leq 63 \text{ s}$
Activation energy: E_a	0.06606	eV	
Boltzman constant: k_B	8.617e-5	eV/K	
			Mean junction temp.: $32.5 \text{ }^\circ\text{C} \leq T_{jm} \leq 122 \text{ }^\circ\text{C}$

For device lifetime estimation the SKiM 63 lifetime model from Semikron is used [63]. The model is using the LESIT lifetime model as a base-line [61]. Based on the simplified assumption of uniform failure mechanism over the entire temperature range, the B10 power cycle (90% of sample components fail if power cycles reach this value) is introduced in [63]. The experimental conditions on which the model relies, are presented in Table 2-5.

The used model can be seen in (2.20) and it includes the dependencies on: wire bond aspect ratio (ar), load pulse duration (t_{on}) and on the freewheeling diode chip thickness (d_{Diode}).

The lifetime equation which expresses the number of cycles to failure (N_f) is described by (2.20).

$$N_f = A \cdot \Delta T_j^\alpha \cdot \exp\left(\frac{E_a}{k_B \cdot T_{jm}}\right) \cdot ar^{\beta_1 \cdot \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{\text{on}}^\gamma}{C + 1}\right) \cdot d_D \quad (2.20)$$

Moreover, Table 2-5 presents the parameters values used in the lifetime-model.

According to the Miner's rule [64], the Lifetime Consumption (LI) is defined as the device accumulated damage which is linearly dependent on the contributions of each thermal cycle and it can be expressed as:

$$LC = \frac{n_{\Delta T1}}{Nf_{\Delta T1}} + \frac{n_{\Delta T2}}{Nf_{\Delta T2}} + \dots + \frac{n_{\Delta Tn}}{Nf_{\Delta Tn}} \leq 1 \quad (2.21)$$

Where: $n_{\Delta Tn}$ – is the number of cycles at the stress ΔT_{Jn} , $Nf_{\Delta Tn}$ – is the number of cycles to failure according to the lifetime-model for the stress ΔT_{Jn} .

Is assumed that when the accumulated damage is one the device fails. The total number of cycles ($n_{\Delta Tn}$) for a specific stress (ΔT_{Jn}) is determined by using the rain-flow counting method according to [65].

2.5 Translation from Detailed Simulation Model to Long Term Simulation Model

The obtained results from this section are presented in P. III.

A Detailed Simulation Model (DSM) of the proposed grid connected PV-inverter and the electro-thermal model has been performed in Matlab/Simulink by considering the aforementioned specifications. Due to the high-level increased complexity of the DSM, the simulation time is much higher than the real time so it takes around 1 s to simulate 10 ms. Another main drawback is the high amount of data generated during the simulation. Due to this the simulation runs out of memory in around 30s real time, which makes it impossible to be used for a long term simulation operation e.g. in one year.

Therefore in order to enable an accurate translation of the one year real field mission profile data (G and T_a) to the device level thermal loading, an accurate and simplified Long Term Simulation Model (LTSM) is recommended.

To overcome this problem an LTSM based on Lookup Tables (LT) which relies on the Detailed Simulation Model (DSM) obtained data has been developed. The LTs are generated by running the DSM under various operating conditions. According to Figure 2-13, the DSM is divided into two main parts. The first one (Figure 2-13 a) is responsible for the translation from the MP (G and T_a) to the converter current (I_c) and DC-link voltage ($V_{DC-Link}$). In order to achieve this it consists of the PV-panel/ MPPT-model. The behavior of this model can be reproduced by two LTs: one for I_c and one for $V_{DC-Link}$. The minimum and maximum values for G and T_a are considered when building the LTs.

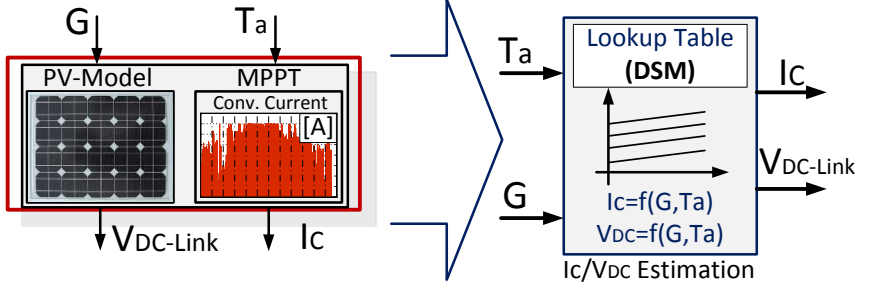
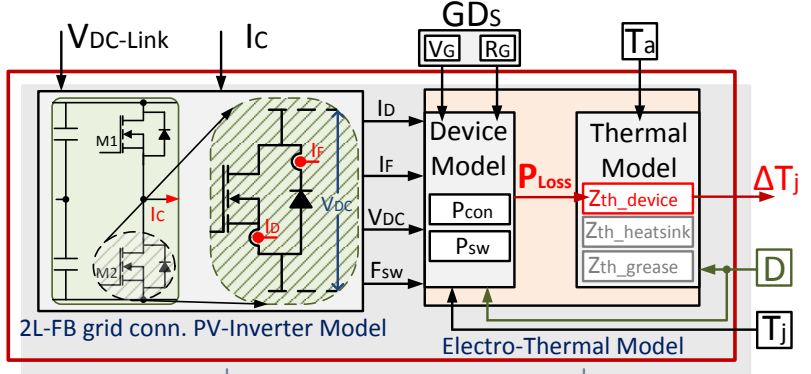
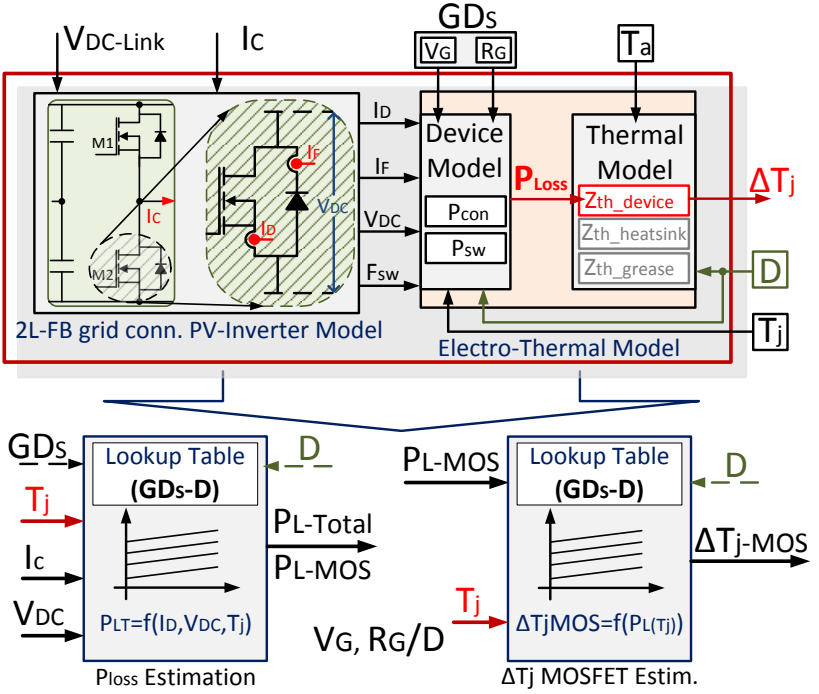

 (a) From MP to I_c and $V_{DC-Link}$

 (b) From I_c and $V_{DC-Link}$ to P_{loss}

 (c) From P_{loss} to ΔT_j

Figure 2-13 Proposed lookup table-based simulation tool when converting from detailed simulation model (DSM) to long term simulation model (LTSM).

Afterwards, the model accuracy is defined by the number of values used from the defined G and T_a interval. By using 40 values for G and 4 values for T_a an accuracy of 98% has been reached. Finally the number of simulations (LTvalues) required to build the LT is equal to:

$$LTvalues = Gvalues \times T_a values \quad (2.22)$$

The model estimates the device losses by considering the converter current (I_c), DC-link voltage ($V_{DC-Link}$) and device junction temperature (T_j) for a specific gate-driver strategy (GDs) and degradation level (D) of

the power device.

The second part (Figure 2-13 b) is responsible for the translation from the converter current (I_C) and DC-link voltage ($V_{DC-Link}$) to the device level power losses and (Figure 2-13 c) temperature swing by considering the GD-parameters, device aging and junction temperature feedback loop. To achieve this, as shown in Figure 2-13 (b), this part consists of the 2L-FB inverter model and the device electro-thermal model.

The behavior of this model can be reproduced by using two LTs.

As shown in Figure 2-13 (b) and (c), two LTs are used to reproduce this behavior. The first one (Figure 2-13 (a)) is making the translation from the converter current and voltage to the device power losses and the second one (Figure 2-13 (b)) from the power losses to the device junction temperature swing (DT_j). Moreover, the model considers also the impact of junction temperature and device aging.

The minimum and maximum values for $I_C - V_{DC-Link}$ pairs and T_j are also considered when building the LTs. Afterwards, the model accuracy is defined by the number of values used from the defined intervals. To achieve a target accuracy of 98%, a number of 52 $I_C - V_{DC-Link}$ pairs and 18 values for T_j have been used for the look-up tables.

By using the $I_C - V_{DC-Link}$ interval pairs (defined from the previous LTs) and the device T_j interval (between minimum and maximum allowed values), the number of simulations required (for one GDs and one D) to build one LT is:

$$LTvalues(GDs1, D1) = (I_C, V_{DC})values \times T_j values \quad (2.23)$$

Therefore, considering n gate-driver strategies (GDs) and m degradation levels (D), a total number of $n*m$ LTs have to be used. In Figure 2-14 it can be seen that depending on the GDs applied and on the

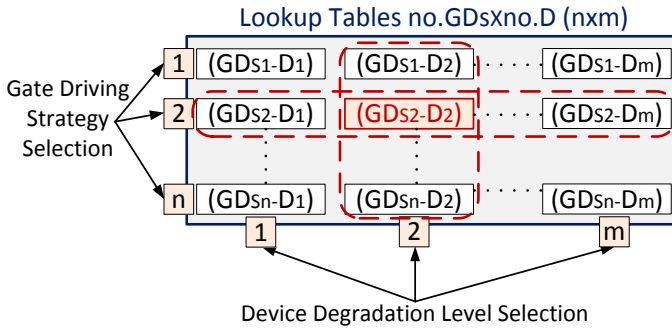


Figure 2-14 Lookup Table selection according to GDs and device degradation variation.

device degradation level, a specific LT is selected. Therefore the model is able to consider the gate driver parameters variation and the device degradation impact on the PV-inverter devices lifetime.

An analytical model which enables the estimation of the thermal profile from the power loss profile is further proposed. The model considers the impact of the thermal impedance (including the thermal capacitance response C_{th}) of the device ($Z_{th_{jc}}$), thermal grease ($Z_{th_{ch}}$) and heatsink ($Z_{th_{ha}}$) by considering the power loss dissipation (device power losses P_{L-MOS} and total converter power losses $P_{L-Total}$) variation with a time-step equal with the mission-profile sampling time of the measured data (T_s). As shown in Figure 2-15, the model considers the previous and actual dissipated power (P_{n-1} , P_n), the time for which the power is applied (t_{n-1} , t_n), the thermal resistance (R_{th}) and time response of the material layers (τ).

The general equation of the model which consists of all the above mentioned parameters is presented in (2.24). The proposed model is used for estimating the temperature drop across the: junction-to-case of the device (ΔT_{j-c}), case-to-heatsink thermal grease (ΔT_G) and heatsink-to-ambient (ΔT_H). Finally, by adding the estimated temperatures (ΔT_H , ΔT_G , ΔT_{j-c}) together with the internal ambient temperature of the converter (T_{ic}), the junction temperature of the device is estimated ($T_{J-MOSFET}$) and used as a feedback in the model (Figure 2-16).

$$\Delta T_{n-1} = P_{n-1} \cdot R_{th} \cdot \left(1 - e^{-\frac{t_{n-1}}{\tau}} \right)$$

$$\Delta T_n = \Delta T_{n-1} \cdot e^{-\frac{t_n - t_{n-1}}{\tau}} + P_n \cdot R_{th} \cdot \left(1 - e^{-\frac{t_n - t_{n-1}}{\tau}} \right)$$
(2.24)

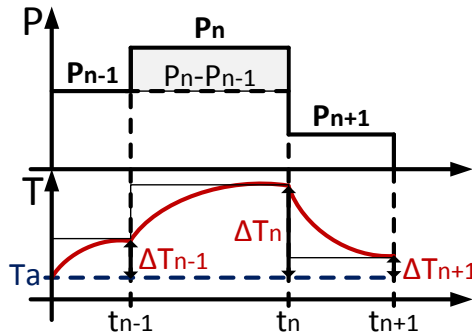


Figure 2-15 Conversion from power losses to temperature.

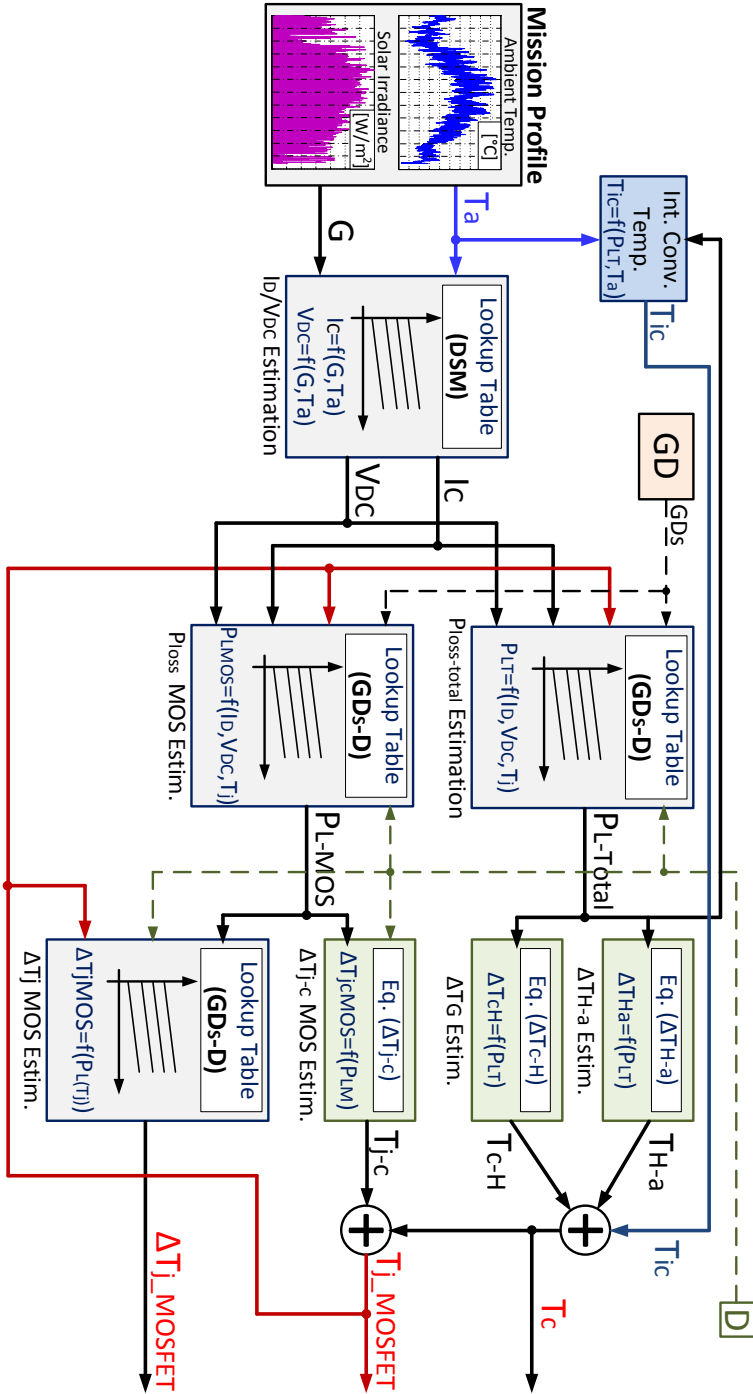


Figure 2-16 Proposed long term simulation model structure.

It is worth to mention that the LTSM includes also a model which takes into consideration the internal temperature of the converter (T_{ic}) as a function of the power loss dissipation and ambient temperature.

Finally, the proposed LTSM structure has been implemented according to Figure 2-16 by considering all the above mentioned conditions, where it can be differentiate the process flow from MP $\rightarrow I_c$ and $V_{DC} \rightarrow P_{L-Total/MOS} \rightarrow T_{j_MOSFET}$. Additionally the impact of gate-driver (GD) and the device aging (D) are also included.

2.6 Summary

In this chapter, the description of the modeling phase of the proposed reliability oriented design tool has been performed.

In this context the chapter has presented the detailed modeling process of the tool, starting with the modeling of the mission-profile (for soft and harsh environmental operating conditions) and of the grid-connected PV-inverter, continuing with the device electro-thermal modeling and ending with the device lifetime model.

Moreover, an accurate translation of the real field mission profile to the device level thermal loading for one-year operation has also been done by developing the long term simulation model.

Chapter 3 Model Validation and Lifetime Analysis of SiC- based PV-inverter Devices

This chapter presents the electro-thermal model validation and the reliability studies performed by the proposed reliability oriented design tool. The chapter is divided into three main sections. In the first section is presented the SiC-based PV-inverter selection, starting with the PV-inverter complexity, continuing with the device electro-thermal modeling of the selected PV-inverter topologies and ending with a hardware cost analyzes of the selected SiC-based PV-inverter. The second section presents the electro-thermal model validation at device level and at system level operation. The last section introduces a novel concept of assessing the reliability of power semiconductor devices by considering the device degradation and the mission profile operating conditions.

3.1 SiC-based PV-inverter selection

The results presented in this section have been presented in P. V and P. VII.

The recent developments in wide band-gap devices based SiC is showing a high impact on the PV-inverter technology, which is strongly influenced by efficiency, power density and cost. Besides the high efficiency of the PV-inverters, also the mechanical size, the compactness, the simple structure and the reliability have an important role in the cost reduction. A typical grid connected PV-system consists of: the voltage source inverter (VSI), the output LCL-filter and the PV-strings. The boost-converter stage (between the PV-strings and inverter) is optional and depends mainly on the PV-system power.

The use of high-efficiency and reliable inverters is a must in order to achieve the price reduction of PV-system technology.

For Si-based PV- inverters, the switching frequency is limited (typical to 16 kHz) by the switching losses leading to increased magnetics, DC-link capacitance and also cooling requirements [66, 67].

3.1.1 PV-inverter complexity

To increase the efficiency of PV-systems, most of the solutions for Si based PV-inverters have moved to three level 3L-structures reaching typical efficiencies up to 96% due to low switching losses of 600V Si IGBT or MOSFET and reduced core losses in the filter. The three level diode neutral point clamping (3L-DNPC) inverter is a good option as it enables the use of lower voltage rated switches (600 V) and also reduces the filtering requirements [66]. This PV-inverter topology (Figure 3-1 a) is eg. used by Danfoss Solar in their products.

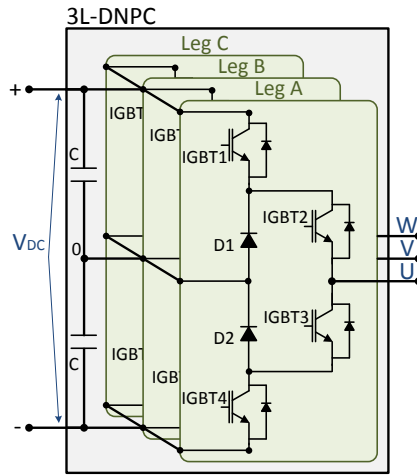
The introduction of SiC devices enables higher blocking voltage capabilities and lower switching losses when comparing to Si-switches. In order to take the advantage of these properties, the three level bipolar-switch neutral point clamping (3L-BS NPC) topology (Figure 3-1 b) has been proposed as a dedicated topology for SiC-devices. In order to reduce the overall costs of the converter, the clamping to the neutral point is achieved by using Si-IGBTs. The companies already started to produce 3L-BS NPC PV-inverters based on SiC-devices for the main switches and Si-IGBTs for the neutral point clamping switches (ex: SMA with STP 20000TLHE-10) [14], [15].

As a consequence of using SiC-devices, the SMA PV-inverter has achieved the highest efficiency on the market (98.5 %) [15]. Even the converter has a high efficiency, the main disadvantage is the higher cost when compared to Si-based PV-inverters. In order to reduce the overall cost, the return to two level full bridge 2L-FB (Figure 3-1 c) with a split capacitor has been proposed as an alternative in this project. With the appearance of 1200V SiC-MOSFETs, it becomes possible to return to a simpler 2L-structure (Figure 3-1 c) with a comparable efficiency but with a high potential to reduce the overall cost.

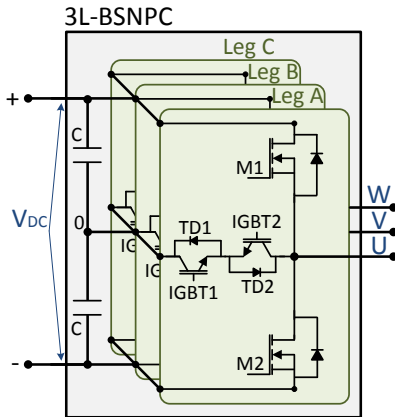
Table 3-1 presents a comparison of the above mentioned PV-inverter topologies: 3L-DNPC (based on Si-IGBTs), 3L-BS NPC (based on SiC-MOSFETs for the main switches and Si-IGBTs for the clamping

to the neutral point) and 2L-FB with split capacitor (based on SiC-MOSFETs). The main disadvantages of the 3L-topologies (3L-DNPC and 3L-BS NPC) when compared to 2L-topology are the increased hardware and control complexity, the double count of switches associated with the drive and protection circuitry, the uneven switch stress and the need for a voltage balancing loop. [68]

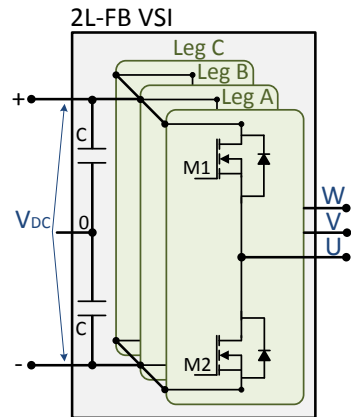
Moreover, 3L-topologies exhibit problems such as unequal loss distribution within the devices, which may lead to unequal temperature distribution. All this will have a negative impact seen from a reliability standpoint.



(a) Si-based 3L-DNPC topology



(b) SiC/Si-based 3L-BS NPC topology



(c) SiC-based 2L-FB topology

Figure 3-1 Three-phase PV-inverter topologies: 3L-DNPC (a), 3L-BS NPC (b) and 2L-FB (c)

Table 3-1 Comparison between 3-phase PV-inverter topologies using Si and SiC technologies

	<i>Three-Phase PV-Inverter Topologies</i>		
	<i>3L- NPC Si</i>	<i>3L-BSNPC SiC-Si</i>	<i>2L-FB SiC</i>
<i>Switches</i>	12 + 6 diodes ☹	12 ☹	6 ☹
<i>Gate Drivers</i>	12 ☹	12 ☹	6 ☹
<i>PWM Algorithm</i>	Complex ☹	Complex ☹	Simple ☹
<i>PCB Size (L x l)</i>	Higher ☹	Higher ☹	Lower ☹
<i>Output Filter Size</i>	Decreased ☹	Decreased ☹	Decreased ☹
<i>THD</i>	Decreased ☹	Decreased ☹	Increased ☹
<i>Efficiency</i>	Moderate ☹	Higher ☹	Higher ☹
<i>Size and Weight</i>	Higher ☹	Moderate ☹	Lower ☹
<i>Switch Stress</i>	Uneven ☹	Uneven ☹	Even ☹
<i>DC-Link Balancing</i>	Needed ☹	Needed ☹	Not needed ☹
<i>Operating Temperature</i>	Low ☹	High ☹	High ☹
<i>DC-Link Cap. Bank</i>	Bigger ☹	Moderate ☹	Smaller ☹
<i>Protection</i>	Complex ☹	Complex ☹	Simple ☹

3.1.2 Thermal loading comparison of the selected topologies

The simulation of each topology has been performed by considering the rated injected power to the grid and the heatsink temperature to a maximum allowed limit of 60 °C.

In these conditions it could be seen the maximum junction temperature of the devices used in the PV-inverter.

A thermal loading comparison of the PV-inverter devices has been done by considering the system specifications from Table 3-2 in the simulation. The converter modeling and control has been presented in Section 2.2. Moreover, a more detailed description of the grid connected PV-inverter in terms of LCL-filter calculation, heatsink thermal impedance and control design has also been presented in P. V.

The model is used to estimate the realistic device (MOSFET and diode) loading current (I_M or I_D) and voltage variations (off-state voltage V_{DC}). All this are further used in the proposed electro-thermal model to estimate the device junction temperature.

Figure 3-2 presents the thermal loading distribution of the converter devices (for all three topologies) when the rated active power is injected into the grid. To determine the maximum junction, the heatsink of the converters has been calculated in order not to overpass the maximum temperature of 60 °C. The simulation has been performed by considering the electro-thermal model from chapter 2.

Table 3-2 PV-system design ratings

2L/3L PV-inverter Specifications			
Rated power	S=25 kVA		
Conv. Output phase voltage	$V_N = 230 \text{ V (RMS) (325 V peak)}$		
Max. Output current	$I_{\max} = 37 \text{ A (RMS) (52 A peak)}$		
Max. DC-link Voltage	$V_{DC-\max} = 1000 \text{ V}$		
Switching Frequency	3L-DNPC	3L-BS NPC	2L-FB
	$f_{sw} = 16 \text{ kHz}$	$f_{sw} = 50 \text{ kHz}$	$f_{sw} = 50 \text{ kHz}$
Heatsink thermal resistance			
Thermal Impedance	Si-based 3L-DNPC	Si/SiC-based 3L-BS NPC	SiC-based 2L-FB
	$R_{th}=0.11 \text{ K/W}$ $\tau= 600 \text{ [s]}$	$R_{th}=0.11 \text{ K/W}$ $\tau= 600 \text{ [s]}$	$R_{th}=0.13 \text{ K/W}$ $\tau= 570 \text{ [s]}$
Device Power Ratings			
Device Type	Single-Phase IGBT module Infineon: F3L50R06W1E3_B11	Discrete IGBT Infineon: IKW50N60T	3-Phase MOSFET module CREE: CCS050M12CM2
Power Ratings Voltage/Current	$V_{(BR)CE}=600 \text{ V}$ $/ I_C=50 \text{ A}$	$V_{(BR)CE}=600 \text{ V}$ $/ I_C=50 \text{ A}$	$V_{(BR)DS}=1200 \text{ V}$ $/ I_D=52 \text{ A}$
Max allowed. J/C Temperature	$T_J= 135 \text{ }^\circ\text{C}$ $T_C= 80 \text{ }^\circ\text{C}$	$T_J= 135 \text{ }^\circ\text{C}$ $T_C= 100 \text{ }^\circ\text{C}$	$T_J= 150 \text{ }^\circ\text{C}$ $T_C= 90 \text{ }^\circ\text{C}$
DC-Link and output filter specifications			
	3L-D NPC	3L-BS NPC	2L-FB
DC-Link Capacitance	32 μF	10 μF	10 μF
Total Filter Inductance	0.52 mH	0.25 mH	0.32 mH
PV-Panel Characteristics-Connection			
PV-Panel Type	ET Black Module (ET-M660250BB)		
Connection Type	Series= 24	Parallel=3	

Figure 3-2 (a) presents the thermal loading of 3L-DNPC converter devices at nominal operating power. As it was expected, the inner IGBT temperature is lower than the outer IGBT temperature. This is mainly due to the current stress distribution and the higher switching frequency of the outer devices. A special attention has to be paid to the NPC diode selection. Beyond the current and voltage ratings capability, the Z_{th_jc} plays a very important role in order to avoid high temperature variations which will have a negative impact from a device reliability standpoint.

The thermal loading of 3L-BS NPC inverter devices is presented in Figure 3-2 (b). In this topology the load current of the NPC freewheeling diode is the same with the clamping IGBT. The most critical component in this specific case is the clamping diode, which has a temperature higher than the IGBT. Although they belong to the same package, their junction temperature differs considerably due to the junction to case

thermal impedance, which in the case of the diode is the double compared to the IGBT. Finally, the thermal loading difference between the devices will have a negative impact on the converter-level reliability [69].

As shown in Figure 3-2 (c), the 2L-FB topology is a good candidate which offers a good thermal loading distribution of the converter devices. The main disadvantages of the converters which rely on this topology are the output filter size and the higher dc-link capacitance. These may be overcome by using SiC-devices, which performs at a higher switching frequency operation compared to the Si-ones. [70] Moreover, once with the increasing of switching frequency lower inductance and capacitance are required. Therefore, film capacitors can be used, overcoming the life-time problem of the electrolytic ones. [71] Another positive fact is that the overall size and weight of the heatsink can also be reduced due to the higher temperature operation capability of SiC-devices. Once with the introduction of SiC devices, the 2L-FB topology is again a good competitor to replace the 3L-ones due to its advantages shown in Table 3-2.

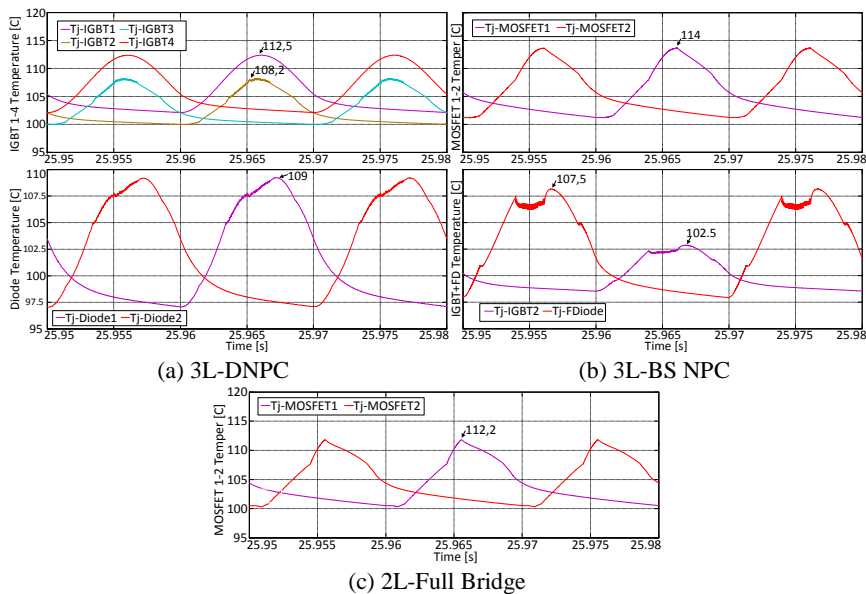


Figure 3-2 Thermal loading distribution across PV-Inverter devices at nominal load operation for: 3L-DNPC (a), 3L-BS NPC (b) and 2L-FB (c)

3.1.3 Cost rentability of the selected SiC-based PV-inverter

To achieve a better selection of the topology, a cost comparison of the PV-inverter topologies has been done and presented in Publication 7.

Finally, to emphasize the cost rentability of the proposed SiC-based 2L-FB topology, a cost-comparison with the Si-based 3L-DNPC has been done by considering the following main components used in a hardware implementation:

- Device Module – Si-IGBT and SiC-MOSFET modules with similar power ratings have been selected. For implementing the 3L-DNPC inverter, three single-phase Si-IGBT modules from Infineon are used. For implementing the 2L-FB inverter, a three-phase SiC-MOSFET module from CREE has been used.
- Gate-Driver (GD) Circuit – the GD circuit is custom made and consists of the following main components: insulated dc/dc converter (Recom Power), linear regulators (Texas Instruments) and GD (Avago Technologies).
- Printed Circuit Board (PCB) – the PCB design has been done in Altium Designer software and it has been produced by PCBCART company. The price of it mainly varies according to the area surface ($L \times l$ [cm²]) and the number of layers.
- Heatsink – The heatsink thermal impedance Z_{th} has been calculated according to the maximum allowed junction and case temperature of the device for the rated power operation. The heatsink has been ordered from HS-Marston company and the price varies according to the cooling method, thermal impedance of the heatsink and the power dissipation.
- DC-Link Capacitor – The DC-Link capacitance has been calculated for a maximum voltage ripple of 5%. It is worth to mention that the capacitance of the SiC inverter is three times lower than for the Si inverter. The capacitors are ordered from Vishay Roederstein manufacturer.
- LCL - Filter – The filter inductance has been calculated for a current ripple of 10 %. The output filter has been custom made by Trafox. The filter inductance of the SiC inverter is with almost 40 % lower compared to the Si solution.

Table 3-3 shows a price comparison of the above mentioned components used in hardware development of the PV-inverters.

Even the price of SiC-MOSFET module is higher than Si-IGBT module, the reduced complexity of SiC-based 2L-FB topology and its higher switching frequency operation (when compared to the Si-based 3L-DNPC topology) have a positive impact on the cost reduction of the PV-inverter.

The overall cost reduction of the SiC-based PV-inverter is achieved due to: the half number of gate drivers, a reduced output filter size (40 % lower inductance), a smaller DC-link capacitance value (70 % lower capacitance) and a smaller PCB dimension. All this will have a positive impact of 9 % in the price reduction of the PV-inverter technology.

As a final conclusion it can be stated that SiC-based 2L-FB inverter is a good candidate to replace the Si-based 3L-DNPC inverter in the application of three-phase PV-inverters for +10 kW range in a cost-effective way. In order to reduce the overall cost and to have a comparable efficiency, this project proposes to use the 2L-FB topology with split capacitor for SiC-based PV-inverter.

Table 3-3 Hardware cost analyzes for two converters

No.	Main Components	Three-Phase PV-Inverter		
		3L-DNPC		2L-HB
		Price [€]	Manufacturer	Price [€]
1	Device Module	(3 x) 60	Infineon IGBT	CREE MOSFET 360
2	Gate Driver Circuit	(12 x) 24.2	Custom made	(6 x) 23.5
3	Printed Circuit Board	23 (30 x 20)	PCBCART Dimension L x l [cm ²]	12.5 (20 x 15)
4	Heat-sink	60	HS-Marston	55
5	DC-Link Capacitors	52	Vishay Roederstein	24
6	LCL-Filter	154	Polylux-TrafoX	102
Total Price:		755.6 €		694.5 €

3.2 Electro-Thermal model validation

The electro-thermal model validation has been done at device level (conduction and switching losses) and at converter level operation through the measured efficiency at different loading conditions.

3.2.1 Device level validation

Conduction losses validation:

To achieve the conduction losses validation, the on-state voltage drop of the device (V_{DS}) is measured by using the Tektronix 371 A curve tracer from Figure 3-3. It is well known that the characteristics of the semiconductor devices are also sensitive to the operating temperature.

In order to perform the temperature dependent characterization, a heating plate is used to control the device temperature.

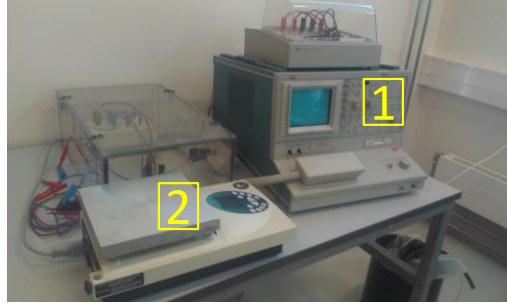
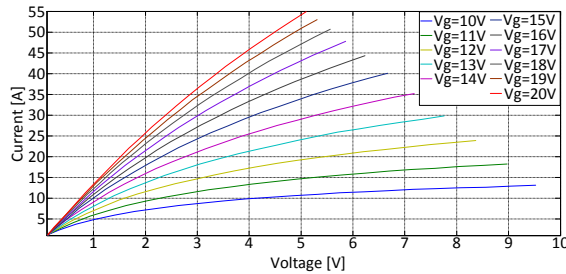
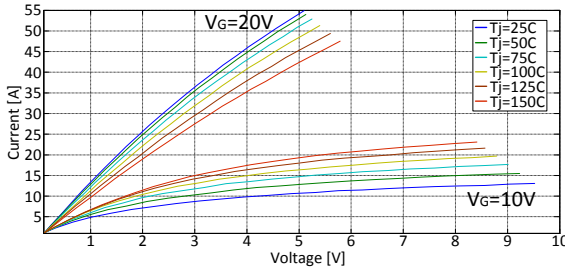


Figure 3-3 Hardware setup for conduction loss characterization: 1 – Tektronix 371A curve tracer, 2 – heating plate.

The obtained results from Figure 3-4 (a) show the MOSFET on-state voltage (V_{DS}) variation with the current (I_D) and gate voltage (V_G) variation. Moreover Figure 3-4 (b) shows the junction temperature impact in the MOSFET on-state voltage drop variation for two gate voltages (10 V and 20 V).



(a) V_G impact in V_{DS-on}



(b) T_j impact in V_{DS-on}

Figure 3-4 Gate voltage impact (a) and temperature variation impact (b) on SiC-MOSFET voltage drop V_{DS} .

In order to calculate the model accuracy, the error between the experimental results and the estimated results is presented in Figure 3-5. It can be noticed that the error is higher at low loading conditions and at higher temperature operation.

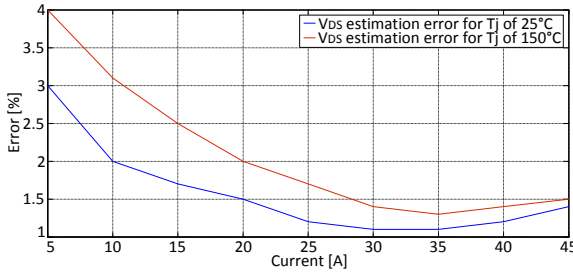
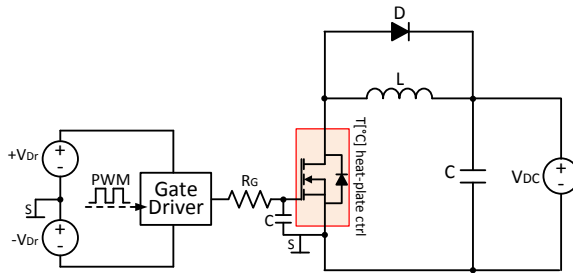


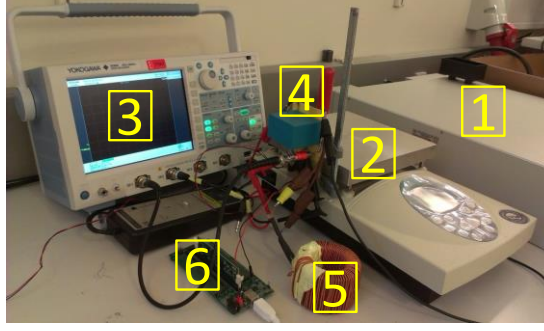
Figure 3-5 Conduction losses estimation error.

Switching losses validation:

An inductive-load Double-Pulse Tester (DPT) has been built to test the switching characteristics of the SiC MOSFET. The schematic and the hardware implementation of the proposed setup are shown in Figure 3-6. The DPT test setup consists of a DSP for control, a heating plate, a power source, an oscilloscope, the load inductor (L) and the DP test board.



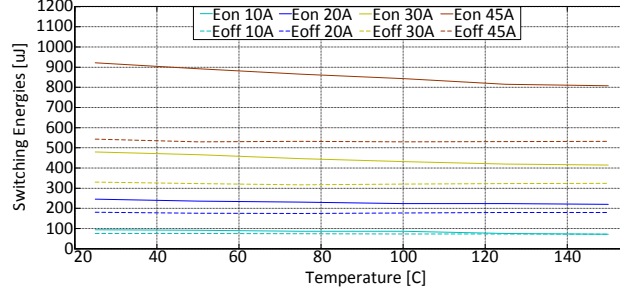
(a) Double-pulse test setup schematic



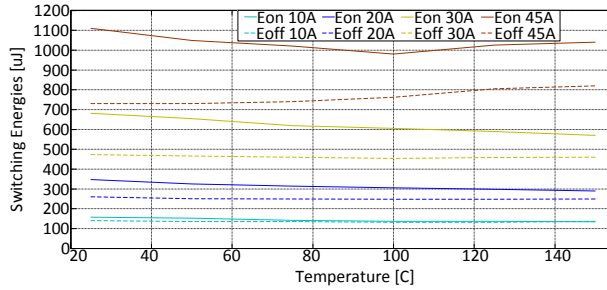
(b) Double-pulse laboratory implementation

Figure 3-6 Double-pulse test-setup schematic (a) and laboratory implementation (b): 1 – DC-power source, 2 – heating plate, 3 – oscilloscope, 4 – double-pulse test board, 5 – load inductor, 6 – DSP control.

The turn-on and turn-off switching energies were measured for the following conditions: $V_{DS}=600$ V, $V_G=+20$ V/-5 V, $R_{G1}=10$ Ω , $R_{G2}=20$ Ω , $I_D=10$ A to 45 A, $T_J=25^\circ\text{C}$ to 150°C . These conditions were considered for two driving resistances of 20 Ω and respectively 10 Ω . The obtained results for both cases are shown in Figure 3-7. In order to validate the switching energies estimation model, Figure 3-8 presents the error between the experimental results and the estimated results.



(a) Esw for $R_G=10$ Ω



(b) Esw for $R_G=20$ Ω

Figure 3-7 Measured switching energies for current variation from 5 A to 45 A, dc-voltage of $V_{DC}=600$ V, $R_G=20$ Ω (a) and $R_G=10$ Ω (b).

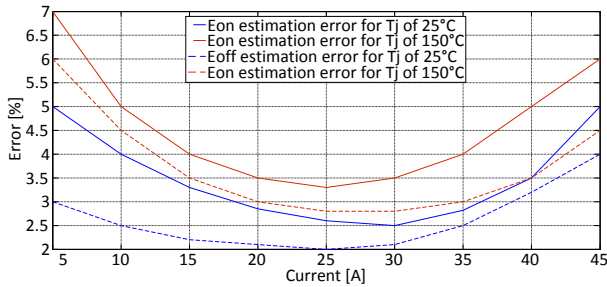


Figure 3-8 Switching energies E_{sw} estimation error.

It can be seen that the error is lower in the middle of the loading operating conditions. Moreover, the estimation error for the E_{on} energies is higher than E_{off} energies. The estimation error depends also on the temperature variation.

The device model validation has been achieved by comparing the obtained simulation results with the experimental values, when applying the same operating conditions. Moreover, the model accuracy according to the loading operation and temperature variation has also been presented.

3.2.2 *Electro-thermal model validation for converter level operation*

The Electro-Thermal model has been validated at system level operation in a grid-connected PV-inverter application. The same conditions were considered for the simulation and for the laboratory implementation. To achieve the model validation, a comparison of the simulation results with the laboratory results has been done.

A schematic of the laboratory setup is introduced in Figure 3-9. The design of a SiC-based 25 kVA grid connected PV-inverter has been performed according to the power rating parameters and specifications given in Table 3-2. A detailed description of the hardware implementation of the 2L-FB inverter has been presented in section 3.1.3.

Figure 3-10 (a) shows the 2L-FB PV-inverter hardware implementation, which can be divided into the following main sections: 1 – 3-phase output power, 2 – DC-input power, 3 – heatsink, 4 – DC - link film capacitors, 5 – device MOSFET module, 6 – gate-driver circuit

and 7 – DSP control.

The PV-inverter devices efficiency (for the CREE-MOSFET power module) is measured for different active power levels injected into the grid, by using the Yokogawa WT3000 power analyzer. The efficiency is measured for power ratings from 0 to 25 kW with load steps of 2.5 kW.

According to the obtained results presented in Figure 3-10 (b), the model is performing a good estimation of the power losses in the whole working area range. The largest power loss deviation from the experimental measurements (being of 7 %) is seen at the lower power operation.

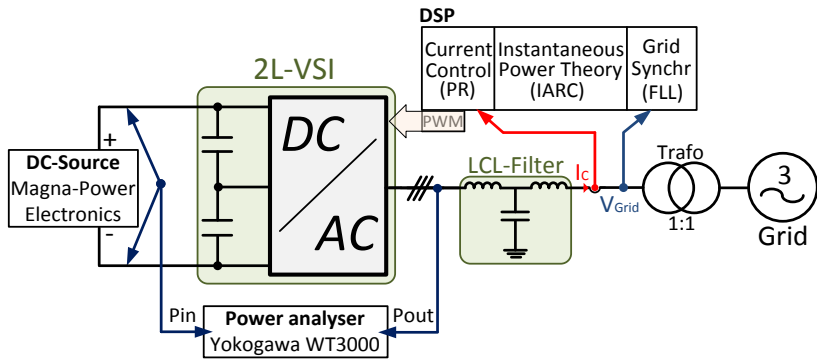
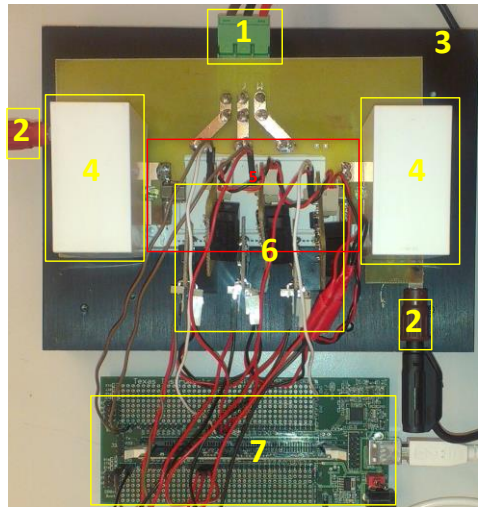
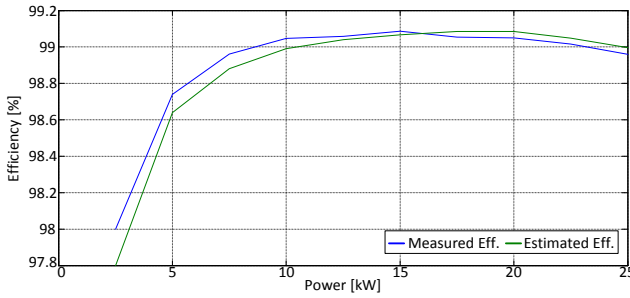


Figure 3-9 Schematics of the laboratory-setup for efficiency testing.



(a) Hardware layout of the SiC-based 2L-FB PV-inverter



(b) Efficiency measurement and estimated curve of the SiC-based 2L-FB PV-inverter

Figure 3-10 Hardware layout (a) and Efficiency curve measured and estimated (b) of the SiC-based 2L-FB PV-inverter: 1 – 3-phase output power, 2 – DC-input power, 3 – heatsink, 4 – DC - link film capacitors, 5 – device MOSFET module, 6 – gate-driver circuit and 7 – DSP control.

3.3 Lifetime analysis of SiC-based PV-inverter devices

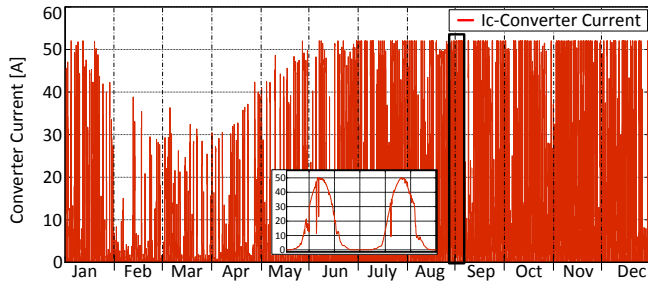
The obtained results from this section are presented in P. II, P. III and P.VIII.

The lifetime of the proposed SiC-based 2L-FB PV-inverter devices is studied. The first part studies the impact in PV-inverter devices lifetime of the MP-variation from soft to harsh operating conditions. In the second part, the impact on reliability of the gate-driver parameters variation in PV-inverter devices is studied.

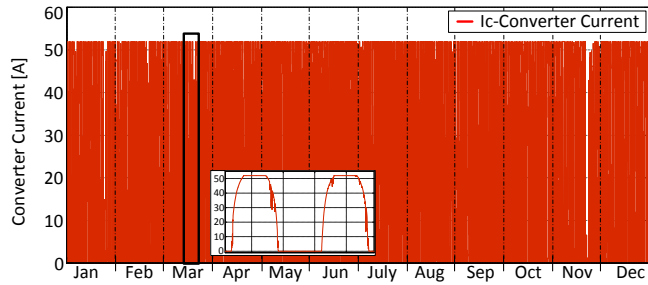
3.3.1 The impact of Mission-Profile variation from soft to harsh operating conditions

In order to evaluate the impact of the MP-variation and device-degradation-aging in the PV-inverter lifetime, the proposed reliability oriented design tool has been used to, considering the above mentioned application specifications.

The proposed LTSM-model has been implemented in order to consider one year measurements of the MP (solar irradiance and ambient temperature) according to the location where the PV-inverter is operating.



(a) Converter current estimation for one year operation in soft-environment conditions (Denmark-Aalborg)



(b) Converter current estimation for one year operation in harsh-environment conditions (USA-Arizona)

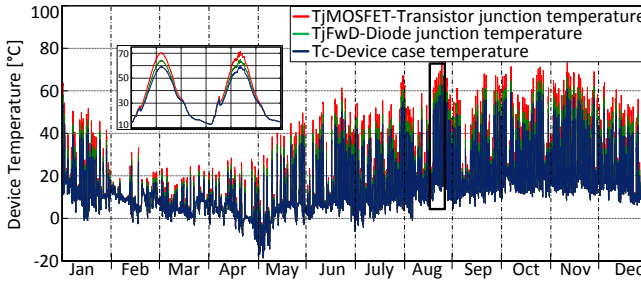
Figure 3-11 Converter current estimation for one year operation in (a) soft-environment conditions (Denmark-Aalborg) and (b) harsh-environment conditions (USA-Arizona).

In order to study the MP-variation impact on the reliability of the PV-inverter devices, the harsh and soft environmental conditions from section 2.1 are selected and considered in the simulation: the first one (soft environment) is from Denmark-Aalborg (Figure 2-2) and the second one (harsh environment) from USA-Arizona (Figure 2-3). The sampling time of the measured data is one minute.

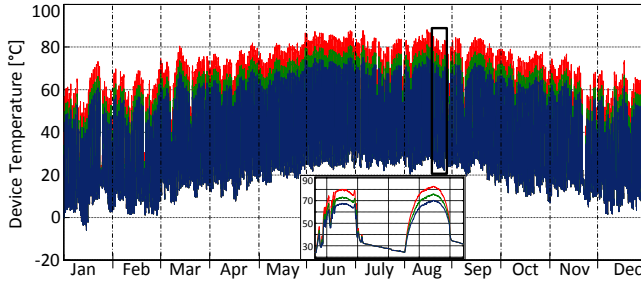
Moreover, to evaluate the impact of the device degradation in the PV-inverter lifetime, the simulation has been performed with and without considering the device aging feedback loop.

The obtained simulation results shows the realistic load current of the converter due to the real field mission-profile applied as an input to the model for one year operation in the soft environment conditions (Figure 3-11 (a)) and harsh environment conditions (Figure 3-11 (b)).

Moreover, by considering the estimated converter current in the model, the thermal loading distribution (in terms of junction and case temperature) of the PV-inverter devices (MOSFET and diode) for the studied cases has been estimated.



(a) Thermal loading of PV-inverter devices for one year operation in soft-environment conditions (Denmark-Aalborg)

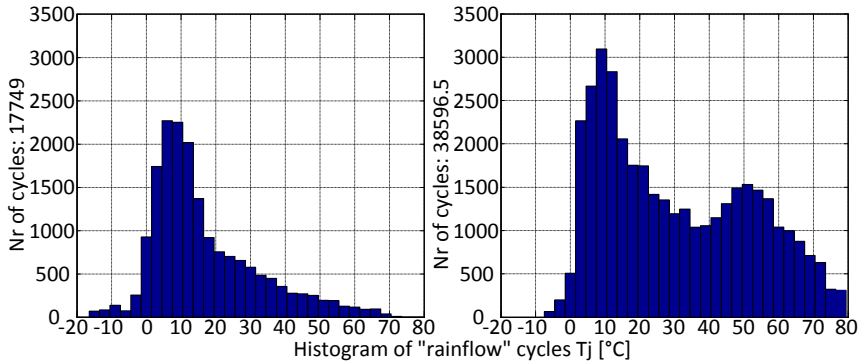


(b) Thermal loading of PV-inverter devices for one year operation in harsh-environment conditions (USA-Arizona)

Figure 3-12 Thermal loading of PV-inverter devices for one year operation in (a) soft-environment conditions (Denmark-Aalborg) and (b) harsh-environment conditions (USA-Arizona).

The obtained one year thermal loading of the converter devices Figure 3-12 has been further used as an input to the lifetime-model presented in section 2.4. As mentioned in section 2.4, for long-term mission profiles, a cycle counting-algorithm is required to exploit the temperature loading profile. For this purpose, a rain-flow counting method algorithm is used and the obtained results (in terms of device thermal-loading distribution) are shown in Figure 3-13 (a) for soft and Figure 3-13 (b) for harsh environmental conditions. It is worth to mention that the estimated no. of cycles has to be multiplied with the MP sampling time T_s (60s) and the no. of cycles per second (50 Hz).

Moreover, Figure 3-14 presents a comparison of the thermal loading between operating the converter in soft and in harsh environmental conditions. The total device accumulated damage has been determined according to Miner's rule [64], with and without considering the device degradation feedback loop in the model. Considering that the device fails when the accumulated damage is 1, the expected PV-inverter devices lifetime is predicted as specified in Table 3-4.



(a) Soft-environment conditions

(b) Harsh-environment conditions

Figure 3-13 Rainflow counting histogram of the PV-inverter devices thermal loading for (a) soft-environment conditions (Denmark-Aalborg) and (b) harsh-environment conditions (USA-Arizona).

The obtained results, shows that the device degradation feedback has an impact from 20 % (for soft environmental conditions) to 30 % (for harsh environmental conditions) in PV-inverter devices lifetime estimation. Therefore, to achieve a correct lifetime estimation it is crucial to consider also the device degradation in the simulation model.

Moreover, the MP-variation from soft to harsh operating conditions has a negative impact of 70 % in the lifetime reduction of the PV-inverter devices.

It can be concluded that the MP-variation of the field where the PV-inverter is operating has a major impact in the converter devices reliability and it should be considered in the design stage in order to better optimize the converter design margin selection.

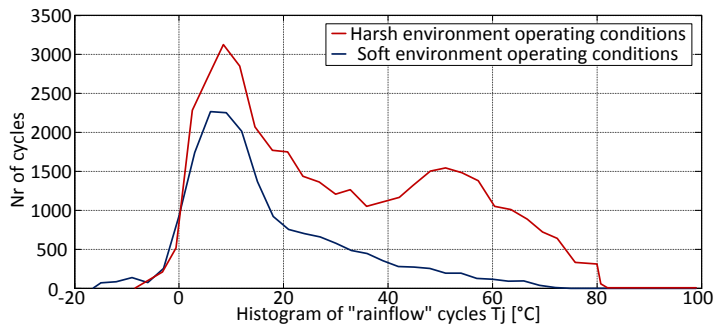


Figure 3-14 PV-inverter devices thermal loading comparison of rainflow counting histogram between soft and harsh-environment conditions.

Table 3-4 MP-variation and device degradation impact on lifetime of PV-inverter devices lifetime

RFMP	Lifetime		Degradation impact in Lifetime	MP-variation (from Denmark to USA) impact in Lifetime
	Without Degradation	With Degradation		
Denmark	16.8 [years]	14 [years]	20 [%]	70 % lifetime reduction
U.S.A.	5.5 [years]	4.2 [years]	30 [%]	

3.3.2 The impact of Gate-Driver parameters variation

It is well known that the gate-driver (GD) parameters (in terms of gate-voltage (V_G) and gate-resistance (R_G)) will influence the conduction and switching losses of the device. Therefore, it is of great interest to study the impact of these parameters on the device lifetime.

Considering the above presented process flow, the reliability-oriented design tool may also be used to study the impact of GD-parameters variation on PV-inverter devices lifetime.

The obtained results presented in Figure 3-15 shows the impact of the GD-parameters (V_G and R_G) in the inverter devices lifetime.

The safe operating area of the device lies between the minimum and maximum allowed gate-driver parameters presented in chapter 4: gate resistance ($R_{G-min} = 10 \Omega$, $R_{G-max} = 70 \Omega$) and gate-source voltage ($V_{G-min} = 10 \text{ V}$, $V_{G-max} = 20 \text{ V}$).

As shown in Figure 3-15, for V_{G-max} (low estimation conduction losses), the variation of R_G has up to 50 % negative impact in device lifetime, from 20 years (GD using V_{G-max} and R_{G-min}) to 9.85 years (GD using V_{G-max} and R_{G-max}).

For V_{G-min} (high conduction losses compared to switching losses), the R_G -variation has a low impact on the devices lifetime, from 0.25 years (GD using V_{G-min} and R_{G-min}) to 0.2 years (GD using V_{G-min} and R_{G-max}).

The obtained results from Table 3-5 shows that depending on the gate-driver strategy, the device degradation may have a negative impact from 28.2 to 34.1 % on the PV-inverter devices lifetime. Therefore, to improve the lifetime estimation accuracy it is important to consider the device degradation in the model.

Another important aspect in the reliability of power devices is the

gate resistance tolerance. According to the datasheet, the typical tolerance error varies from ± 1 to 5 % of the base resistance value. By considering this into the studies it results in a variation on the device reliability of 3 to 8 %.

It can be concluded that the GD-parameter has a major impact on the converter devices reliability. Therefore, special attention has to be paid to the GD-parameters selection for improving the lifetime of the power-devices.

Table 3-5 GD-parameters variation and device degradation impact on PV-inverter devices lifetime

GD strategy (V_G , R_G)		Lifetime [years]		Degradation impact in lifetime
		Without Degradation	With Degradation	
1.	GDs1 (20 V, 10 Ω)	26.4	20.1	28.2 %
2.	GDs2 (17 V, 12 Ω)	13.2	10.2	29.3 %
3.	GDs3 (15 V, 20 Ω)	5.6	4.3	30.1 %
4.	GDs4 (14 V, 35 Ω)	3.4	2.6	31.2 %
5.	GDs5 (12 V, 55 Ω)	1.7	1.3	32.4 %
6.	GDs6 (10 V, 70 Ω)	0.2	0.2	34.1 %

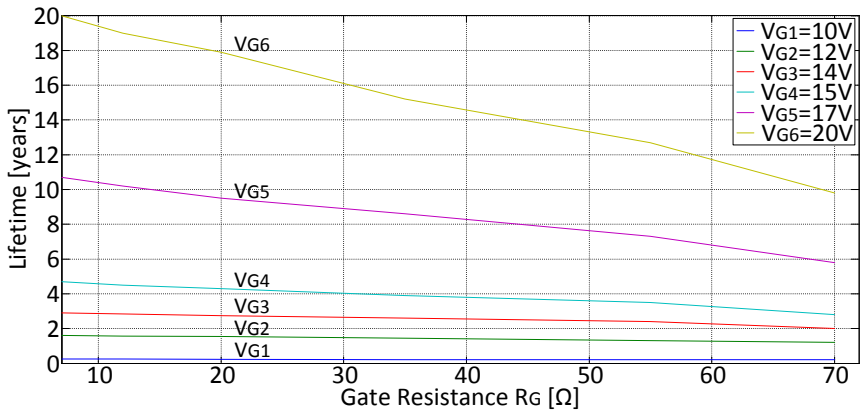


Figure 3-15 GD-parameters (V_G and R_G) variation impact in PV-inverter devices lifetime

3.3.3 The impact of Mission-Profile sampling-time in the lifetime estimation accuracy

The estimated lifetime accuracy depends on the reliability oriented design tool accuracy and on the MP sampling time. Lower T_s gives a higher estimated lifetime accuracy and also a longer simulation time.

Therefore, a method to determine the optimum T_s is of interest.

In order to perform the lifetime-estimation sensitivity to the MP sampling-time variation, the MP from Aalborg-Denmark is used. The MP is measured at Department of Energy Technology (Aalborg University) and the sampling time of the data (G and T_a) is $T_s=200$ ms.

It is well known that by decreasing the sampling-time, the number of data increases, thus the simulation time increases. It has been determined that a long term simulation of one week with a MP sampling time of 1 s, is the maximum allowed data for the computer in order to avoid the out-of-memory situation. Moreover, the simulation takes much longer time compared to the situation when the MP sampling time of 1 minute is used. Therefore, it has been decided that the minimum MP sampling time of 1 second and the long term MP of one week operation is considered into the studies.

Seven MP sampling times from 1s to 5 minutes were tested with the proposed reliability oriented design tool by considering the systems specifications of the SiC-based 2L-FB PV inverter presented in section 2.2. According to the obtained results presented in Figure 3-16, it can be seen that when T_s increases, the lifetime estimation accuracy decreases. When $T_s=5$ min is used, the lifetime estimation error is 28% (when using $T_s=1$ s as the reference value). It can also be clearly seen in Figure 3-16 that a T_s lower than 30 s does not have a significant impact on the lifetime estimation accuracy.

Therefore as a compromise between the simulation time and the lifetime-estimation accuracy, a mission-profile sampling time of 30 s could have been selected.

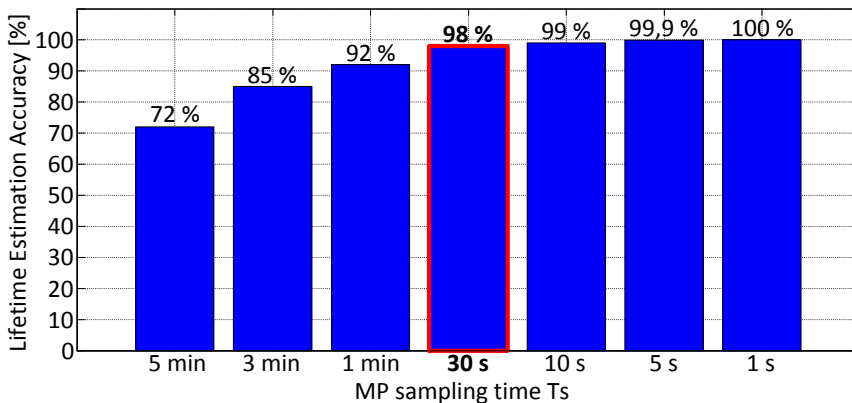


Figure 3-16 The lifetime estimation accuracy introduced by the MP sampling time variation.

3.4 Summary

In this chapter, the electro-thermal model validation and the complex reliability studies have been performed.

In this context the electro-thermal model validation has been achieved for device-level and converter-level operation. Moreover, a SiC-based 2L-FB PV-inverter has been selected as a study case.

This chapter introduces a novel concept of assessing the devices reliability by considering the mission-profile operating conditions and the device degradation impact.

The proposed tool has been used to perform the PV-inverter devices lifetime analysis and the following results have been obtained:

- Modelling the device degradation has an impact of up to 30% in PV-inverter devices lifetime for the studied conditions.
- The MP-variation from soft to harsh environmental operating conditions has a negative impact of 70 % in the PV-inverter devices lifetime reduction.
- The gate-driver parameters variation has an important impact on the devices lifetime. The gate resistance manufacturer has typically tolerance error of ± 1 to 5 % (of the base resistance value) which introduces a negative impact in the device reliability of 3 to 8 %.
- The MP sampling-time variation has also impact on lifetime-estimation accuracy. The MP sampling time of 30 s has been determined as a compromise between the simulation time and the lifetime-estimation accuracy.

Chapter 4

A Novel Gate-Driver Concept for Enhancing the Reliability of Power-Semiconductor Devices

This chapter presents the modeling, implementation and validation of a novel gate-driver concept for enhancing the reliability of power semiconductor devices and its system. The chapter is divided into four main sections. In the first two sections the advanced gate-driver circuit is modeled and a new method for active-thermal control is proposed. The third section presents the laboratory implementation and validation of the proposed gate-driver concept. The last section proposes an advanced gate-driver strategy for reliability improvement of the PV-inverter devices.

The knowledge gained from the field data and simulations of high power devices concluded that the temperature is one of the most important stressors, which involves failures in the power semiconductor devices. For each 10°C increase in temperature the failure rate is almost doubled. Therefore, the temperature variation of the semiconductor devices plays a key role in the robustness design and reliability of power electronics converters. This factor has a major impact on the power converters used in renewable energy systems, like wind energy and solar energy applications, due to the fluctuating nature in the mission profile (wind, solar irradiance). The introduced converter current changes cause device junction temperature variations (due to the power loss dissipation)

that might reduce the reliability of the semiconductor devices as well as the power electronic systems. By achieving a more constant power loss dissipation (in the semiconductor device), the junction temperature can be kept constant, and thereby enhance the reliability of the power semiconductor devices.

4.1 Advanced Gate-Driver concept

Different Gate-Driver (GD) operating conditions may influence the device losses and thereby temperature-implicitly the device reliability as also discussed previously.

The proposed advanced gate-driving (AGD) concept relates to a method for controlling the device power losses and implicitly the junction temperature, enhancing the reliability of power semiconductor devices used in grid connected PV-inverter applications.

As an example, the SiC-based PV-inverter from Chapter 3 is considered as a study case. The studies rely on the SiC-based MOSFET module used in the previous chapter.

The conduction and switching losses of the device are influenced by the gate driver (GD) parameters: gate voltage (V_G) and gate resistance (R_G). Considering the device intrinsic limits explained in Figure 4-1 (gate-oxide breakdown, thermal runaway, gate ringing and PWM limitations) the allowed V_G and R_G ranges are defined as follows:

- The minimum turn-on gate voltage $V_{G-min}=10$ V is chosen from the typical output characteristic given in the datasheet in order to avoid thermal runaway of the device.
- The maximum turn-on gate voltage $V_{G-max}= 20$ V is provided in the datasheet in order to avoid the gate-oxide breakdown.
- The minimum allowed gate resistance $R_{G-min}= 10$ Ω has been determined experimentally in order to avoid the gate ringing.
- The maximum allowed gate resistance $R_{G-max}= 70$ Ω is determined by considering the PWM-limit.

Considering the PV-inverter specifications introduced in chapter 3, the operating switching frequency of the device is selected to be $f_{sw}=50$ kHz which implies a switching period of $T_{sw}=20$ μ s. By considering that the duty cycle (D) varies from $0.1 \leq D \leq 0.9$, the on-time period of the

device varies as follows:

$$\begin{aligned} 0.1 \cdot T_{sw} &\leq T_{on} \leq 0.9 \cdot T_{sw} \\ 2\mu s &\leq T_{on} \leq 18\mu s \end{aligned} \quad (3.1)$$

Furthermore, the maximum rise/fall time T_{rf-max} of the device current is chosen as one third (33 %) from the minimum turn on-time T_{on-min} :

$$T_{rf-max} = \frac{T_{on-min}}{3} = \frac{2[\mu s]}{3} = 660[ns] \quad (3.2)$$

From the datasheet it is known that for $V_G=10$ V the gate charge is $Q_G = 90$ nC. The gate capacitance C_G has the following value:

$$C_G = \frac{Q_G}{V_G} = \frac{90[nC]}{10[V]} = 9[nF] \quad (3.3)$$

Finally, the maximum gate resistance R_{max} required to turn on/off the device in T_{rf-max} is:

$$R_{max} = \frac{T_{rf-max}}{C_G} = \frac{660[ns]}{9[nF]} \cong 70[\Omega] \quad (3.4)$$

A safe operating area which defines the loss budget of the device (Figure 4-1) lies between the minimum and maximum allowed gate resistance ($R_{G-min}=10 \Omega$, $R_{G-max}=70 \Omega$) and gate-source voltage ($V_{G-min}=10$ V, $V_{G-max}=20$ V).

In respect to the power losses, three main gate-driver operation points (OP) can be defined. The lowest loss operating point and the highest loss operating point are achieved, when GD strategy 0 (lowest loss operating point: V_{G-max} and R_{G-min}) or GD strategy 2 (highest loss operating point: V_{G-min} and R_{G-max}) are used, respectively. The GD strategy 1 is used for the normal operation, where $V_{G-no}=15$ V and $R_{G-no}= 20 \Omega$ are defined according to the loss budget strategy which is detailed explained in section 3.5. For this specific case the GDs 1 operates at the same conditions with the Traditional Gate-Driver (TGD defined by a single operating point). Thus, with respect to the traditional GD (GDs1), the advanced GD strategy offers the possibility to increase (GDs 2) or to decrease the semiconductor device losses (GDs 0) as well. The GDs 2 and GDs 0 define the available loss range, where a regulation strategy can be applied in between.

For instance, but not only, a temperature control could be implemented by linearly varying the gate-driver parameters in the range GDs0-GDs2 to limit the temperature variation.

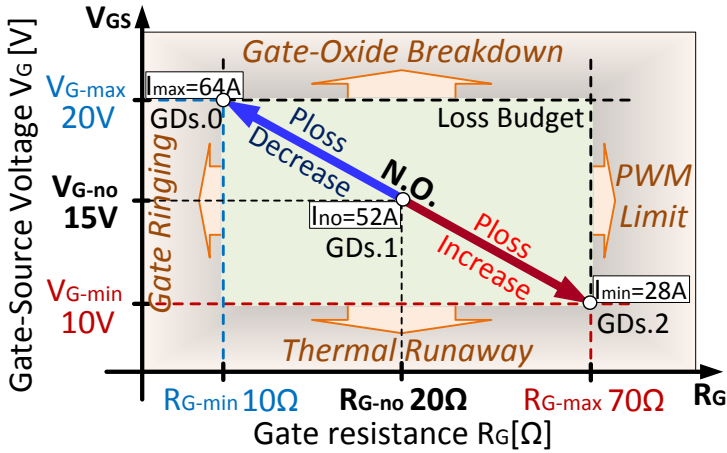


Figure 4-1 Semiconductor devices intrinsic limits and loss budget limits for advanced gate-driver concept.

In Figure 4-2 is proposed an advanced gate-driver concept aimed to change the gate-resistance and gate-source voltage in order to preserve a constant device loss dissipation and thereby also temperature.

As shown to Figure 2-2 the temperature controller will change the gate-driver operation conditions (R_G and V_G values) in an active way, depending on the measured device temperature.

The main objective of the temperature controller is to provide the necessary R_G and V_G values (between the minimum and maximum allowed limits) in order to obtain zero steady state error between the reference and the measured temperature.

According to the temperature error the references of the gate-driver operating condition (R_G and V_G values) are decided in order to keep constant the device losses by considering the loss budget control strategy.

As a result, when the device current increases from I_{no} to I_{max} , (by changing the GD strategy from GDs 1 to GDs 0) the power losses can be preserved almost fixed. On the other hand, if the device current decreases from I_{no} to I_{min} , (by changing the GD strategy from GDs 1 to GDs 2) the power losses of the device are kept constant and the device temperature is not changing.

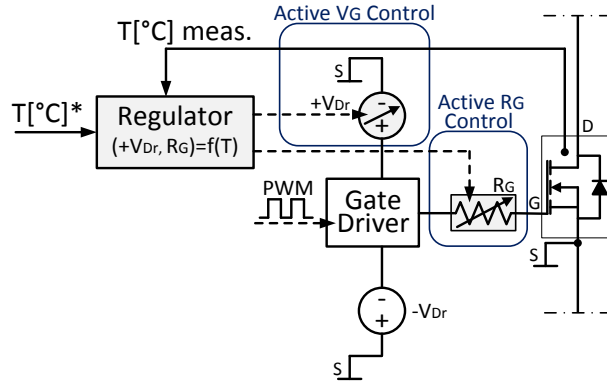


Figure 4-2 Advanced gate-driver for temperature control

4.2 Proposed Advanced Gate-Driver circuit for temperature control of power-devices

A more detailed description and implementation of the proposed advanced gate-driver concept is presented in Figure 4-3. The circuit for the active gate-voltage control and for the active gate-resistance control can be seen.

The advanced gate-driver circuit is used to achieve a temperature-dependent control of the power MOS gate-voltage and gate-resistance. Specifically, the temperature of the power semiconductor switching device is detected and if it is higher (lower) than the reference, the gate-drive voltage is raised (reduced) and the gate-drive resistance value is reduced (increased) until the measured temperature feedback reaches the reference.

The gate-drive voltage and gate-drive resistance values are dynamically controlled according to the error between the reference and the measured temperature of the power semiconductor device.

The main objective of the present idea is to provide a gate-driver circuit, which reduces the dependency of the device power losses variations on the device loading variations and instead is keeping a constant temperature.

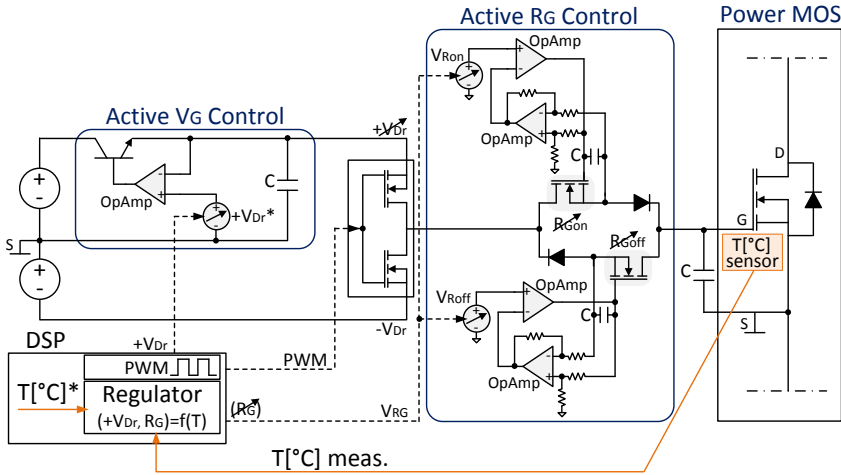


Figure 4-3 The proposed advanced gate-driver circuit design.

4.2.1 Active gate-voltage (V_G) control

The basic idea of the active gate-voltage V_G circuit is illustrated in Figure 4-3. A linear regulator is used to provide a temperature-dependent voltage $+V_{Dr}$ supply for the driver stage.

Figure 4-4 presents the device gate-voltage V_G control of the device along with the variation of the driver voltage $+V_{Dr}$.

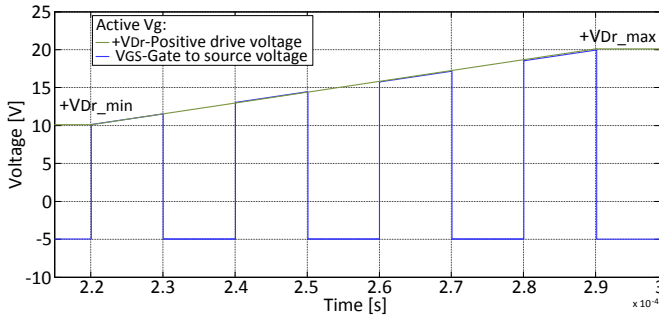


Figure 4-4 Active gate-voltage control by controlling the positive voltage supply.

4.2.2 Active gate-resistance (R_G) control

The transistors are usually used as controlled to be on or off but they can also be used as a controlled variable resistance. When discussing the MOSFET devices the drain-source resistance R_{DS} is a function of

the applied gate-source voltage V_G . Therefore, the device operates as a voltage controlled resistance. Moreover, the MOSFET on – state resistance R_{DS} will play the role of the power MOS gate-resistance R_G . In order to achieve an active control of the gate-resistance R_G for turn-on/turn-off operation, the circuit presented in Figure 4-3 has been proposed.

An accurate control of the rising/falling time of the device current can be achieved for a wide range of values between the minimum and maximum allowed limits, as it can be seen in Figure 4-5.

The active gate-resistance circuit is used to provide a temperature-dependent control of the power MOS gate resistance.

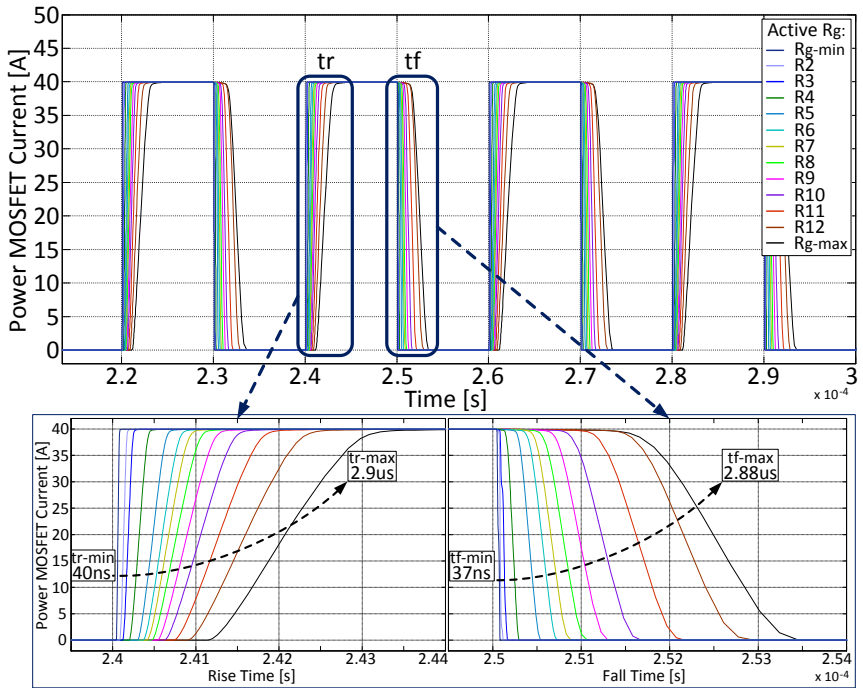


Figure 4-5 Active gate resistance controllability impact on the control of the rise (tr) and fall (tf) time of the device current

4.3 The device active-thermal control based on the Advanced Gate-Driver concept

In order to understand the gate-driving impact on the junction temperature variation control, a comparison between a Traditional Gate-

Driver (TGD) and an Advanced Gate-Driver (AGD) has been performed. According to Table 3-2 it can be seen that the rated power of the 2L-FB PV-inverter is 25 kW and the corresponding maximum peak current is $I_{no} = 52$ A. When the rated active power is injected into the grid and the TGD is used, the maximum dissipated power losses of the inverter devices (one MOSFET+ Fw diode device) is 263 W (43 W per device). The converter has been designed to consider the nominal operation current $I_{no} = 52$ A for TGD operation.

Moreover this establish the inverter maximum allowed dissipated power losses ($P_{L-max} = 263$ W) which defines the thermal system power dissipation limits (heatsink and thermal grease) in order to operate in the Safe Operating Area (SOA) range. If the maximum allowed dissipated power is exceeded, the thermal limitations of the devices are overpassed, and the reliability of the devices may be reduced considerably.

The I_{max} (I_{min}) is defined as the maximum current injected by the inverter for the lowest loss GDs0 (highest loss operating point-GDs1) and not exceeding the maximum allowed dissipated power $\approx P_{L-max}$ (defined by the GDs1=TGD under rated converter current I_{no} operation). Thus the maximum allowed current when the inverter is operating with AGDs is: $I_{max} = 64$ A for GDs0, $I_{min} = 28.5$ A for GDs2 and $I_{no} = 52$ A for GDs1 (TGD).

The advanced driver concept as illustrated in Figure 4-3 is aimed to change the gate resistance R_G and gate-source voltage V_G in order to obtain a constant device loss dissipation.

The proposed active thermal control schematic presented in Figure 4-6 relies on the AGD-concept. Moreover, it can be seen that the proposed control method consists of a PI-controller, which provides the reference gate-resistance (R_G^*) according to the device temperature error.

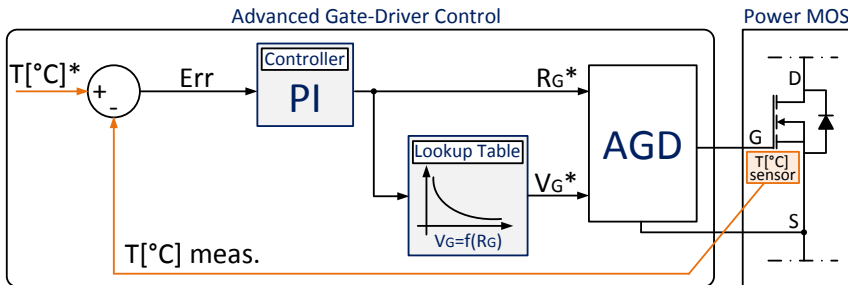


Figure 4-6 Active thermal-control of the power device by using the advanced gate-driver concept

Additionally, the curve-fitting tool from Matlab is used to define the curve equation which express the gate voltage reference (V_G^*) as a function of gate-resistance (R_G^*).

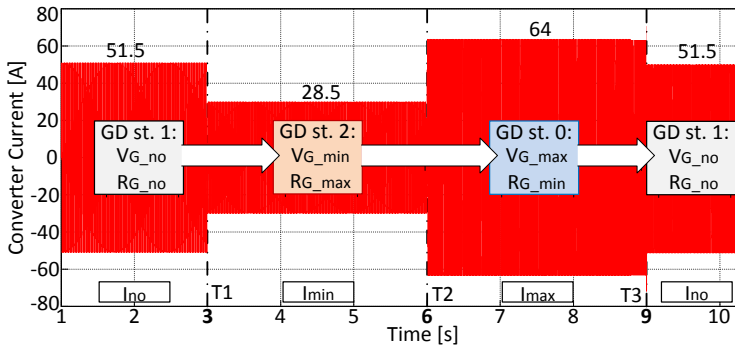
In order to achieve a faster and accurate device temperature control, the PI-controller time response should be lower than the device thermal impedance ($Z_{th_{jc}}$).

To better understand the advanced (AGD) concept strategy and its impact on the junction temperature control the described 2L-FB PV-inverter is operating with the following current variations (Figure 4-7 (a)): from I_{no} (51.5 A) to I_{min} (28.5 A) at time T1 (3 s), from I_{min} (28.5 A) to I_{max} (64 A) at time T2 (6 s) and finally from I_{max} (64 A) to I_{no} (51.5 A) at time T3 (9 s).

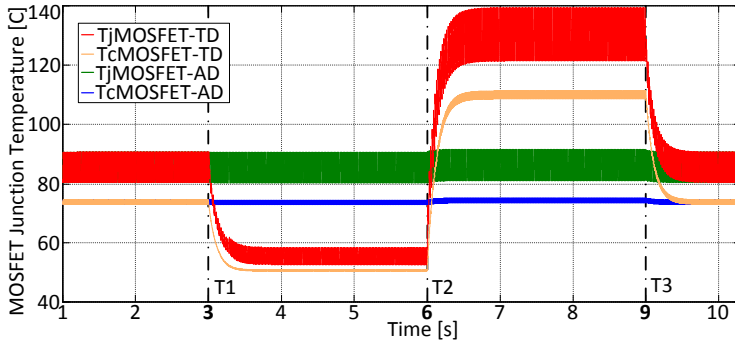
If the traditional gate-driver is used (defined by one operating point) the junction temperature of the device has the behavior shown by the red curve from Figure 4-7 (b). Moreover, the device/converter power losses variation can be seen in Figure 4-7 (c).

If the proposed advanced gate-driver is used, it can be seen that when the load current is changing from I_{no} (51.5 A) to I_{min} (28.5 A at T1), the losses are kept constant due to the temperature controller, which is changing the R_G and V_G values from GDs1 to GDs2, and thereby the device junction temperature is not varying. For the second load step (T2) from I_{min} (28.5 A) to I_{max} (64 A), the GD strategy is changed from GDs2 to GDs0 and thus the device losses are not changing. In the last case scenario (T3), the load current is changed from I_{max} (64 A) to I_{no} (51.5 A). The losses are kept at the same constant value by changing the GD strategy from GDs0 to GDs1.

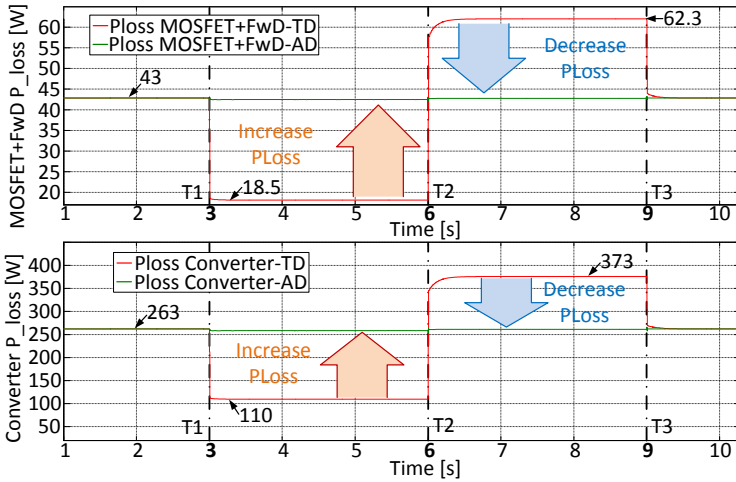
According to the device temperature variation, the gate resistance and gate source voltage are selected in order to keep constant device losses and thereby junction temperature by considering the outlined loss budget control strategy. Depending on the device temperature error, the V_G and R_G may vary between the minimum and maximum allowed limits, so that a high accuracy of the temperature controllability can be achieved by considering the loss budget control strategy.



(a) Current variation of the converter



(b) Junction temperature of the semiconductor device



(c) Power losses of the semiconductor device and of the PV-inverter

Figure 4-7(a) Current variation of the converter, (b) Junction temperature of the semiconductor device, (c) Power losses of the semiconductor device and the PV-inverter module

It can be concluded that by using the proposed advanced gate-driver, the junction temperature can be controlled to the desired refer-

ence value (T^*) during the load changes of the converter, and thus it is expected to improve the device reliability as the temperature variation is reduced significantly.

4.4 Advanced Gate-Driver validation

To validate the proposed advanced GD concept, the circuit shown in Figure 4-8 was considered for a single-phase inverter prototype (Figure 4-9).

As shown to Figure 4-8 the upper device is controlled by a traditional GD and the lower device by using the proposed advanced GD concept. Discrete SiC-MOSFET devices have been used in order to be able to perform a comparison of thermal-loading and also validation of the proposed AGD-concept. Moreover, as shown to Figure 4-8, the control has been performed by using a DSP, a load resistor is used to achieve load current variation and an infrared camera is used for device temperature measurement.

In order to achieve the model validation by using the device active thermal control based on the AGD-concept, the temperature of the lower device should be kept constant at load variations.

The hardware implementation of the proposed AGD is presented in Figure 4-9. The top and bottom-layers of the proposed structure are shown in Figure 4-9.

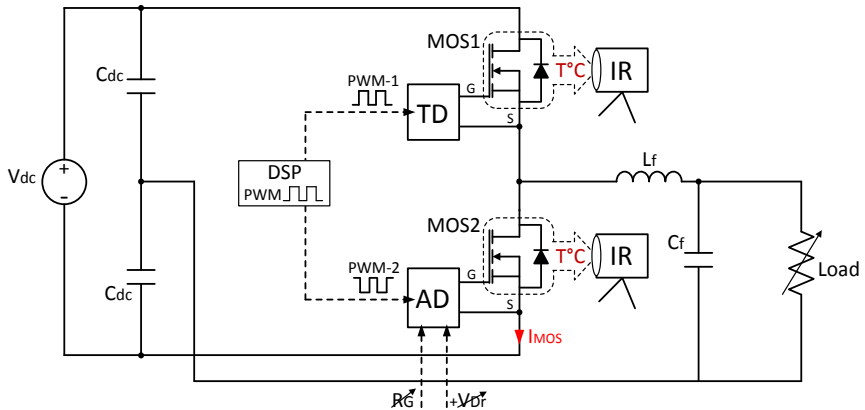


Figure 4-8 Single-Phase inverter topology for studying the new driving concept

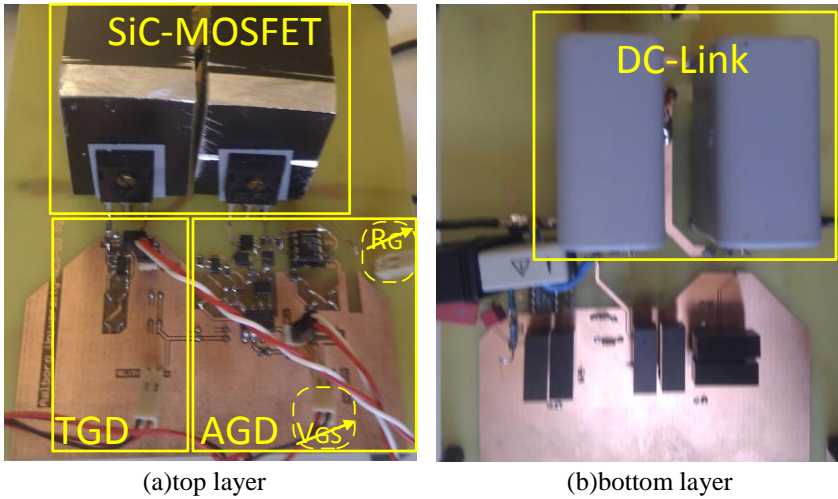


Figure 4-9 Hardware design of the advanced gate-driver to demonstrate the new concept

The advanced gate-driver and the traditional gate-driver implementation, the DC-link capacitors and the SiC-MOSFET devices used in the studies for the proof-of-concept are shown.

A thermal camera is used (Figure 4-10) to evaluate the impact in device temperature control when using the AGD compared to TGD. As seen in Figure 4-10, when using the TGD, the device temperature varies with the load (from $I_1 = 5\text{ A}$ to $I_2 = 10\text{ A}$). As a consequence it can clearly be seen that when using the AGD the device temperature is almost constant even when load variations occur.

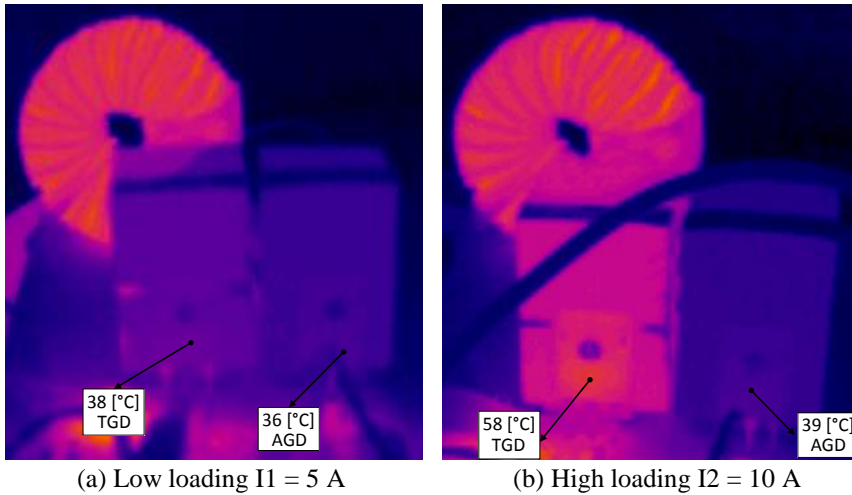


Figure 4-10 The advanced GD impact on the temperature controllability of the power device when the load is changing from (a) $I_1 = 5\text{ A}$ to (b) $I_2 = 10\text{ A}$.

Finally, based on the obtained results it can be stated that the active-thermal control based AGD has been successfully validated.

4.5 Advanced Gate-Driver strategy impact in reliability of the PV-inverter devices

In order to study the AGD impact on the reliability of the proposed PV-Inverter application, a GD control strategy using three main operating points has been proposed: GDs0 ($V_{G0}=20$ V, $R_{G0}= 10$ Ω), GDs1 ($V_{G1}=15$ V, $R_{G1}= 20$ Ω) and GDs2 ($V_{G2}=10$ V, $R_{G2}= 70$ Ω).

Figure 4-11 shows the simulated converter power losses variation, when the current is increased from 0 to 50 A for the proposed AGD operating points. The power loss between GDs0 and GDs2 defines the available power loss regulation range to control the temperature. The GDs1 defines the power loss target. Reporting to this target, the power losses may be increased if the regulation strategy of the GD parameters is controlled in direction of GDs2, or decreased if the GD parameters are controlled in direction of GDs0. Therefore the GDs1 operating point is selected according to the desired positive and negative power loss reserve of controlling the temperature.

A gate-driving selector model has been proposed according to Figure 4-11. The model optimizes the gate driving strategy selection in order to achieve minimum power loss changes when the load current variations occur. Let's assume that the converter current is changing from operating point 1 ($I_1 = 40$ A) to operating point 2 ($I_2 = 23$ A). If the GDs1 is used for I_1 , the power loss is PL1. This defines the power loss target (PL1) for the operating point 2. Therefore, in order to minimize the power loss changes, the GDs which provide the closest loss value with the target (PL1) is selected for the second operating point (GDs2 for this case). Afterwards, the GD parameters are changed from GDs2 to GDs1 in a specified time.

The same process applies, when the converter current is changed from low current $I_2 = 23$ A to high current $I_1 = 40$ A. For this case, when using the GDs1 for I_2 , the power losses are PL2. Therefore, in order to keep the loss constant (PL2) even at load variation from I_2 to I_1 , the driving strategy is changing from GDs1 to GDs0.

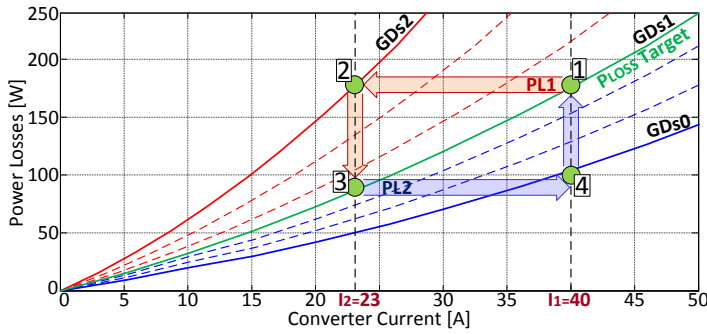


Figure 4-11 Advanced GD control-strategy impact in converter devices power losses when the following strategies are considered: GDs0 ($V_{GS0}=20$ V, $R_{G0}=7$ Ω), GDs1 ($V_{GS1}=15$ V, $R_{G1}=20$ Ω), and GDs2 ($V_{GS2}=10$ V, $R_{G2}=70$ Ω).

Afterwards, the GD parameters are changed from GDs0 to GDs1 in a specified time.

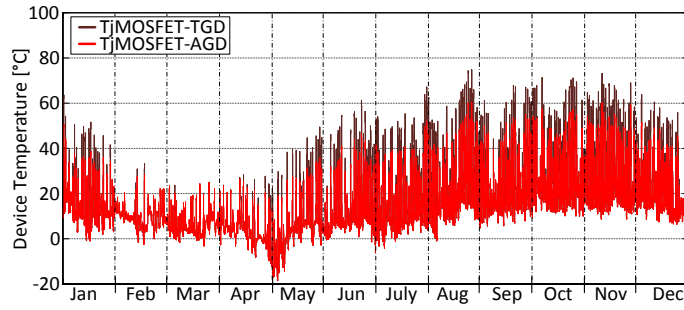
Therefore, it can be seen from the example that GDs1 defines the power loss target, which has to be reached at any load changes. In the driving strategy GDs0 and GDs2 is defined the maximum available positive and negative power loss reserve for controlling the temperature.

In order to study the impact of the AGD on the lifetime of the PV-inverter devices, the above mentioned control strategy has been implemented in the proposed reliability oriented design tool from Chapter 2. Moreover, the one year simulation (with the soft and harsh mission-profile operating conditions) has been performed by considering the conditions defined in Chapter 3.

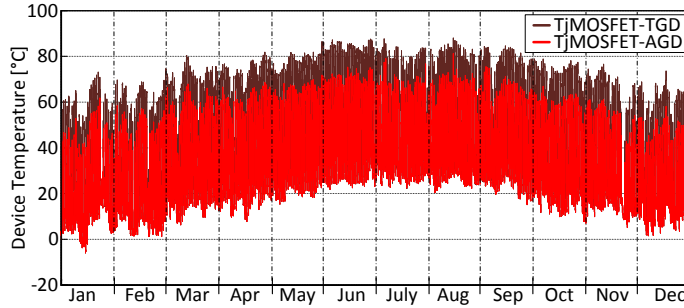
In this context, a comparison between the thermal loading distribution of the converter devices has been performed (in terms of mean T_j (Figure 4-12)) considering the AGD strategy operation versus the TGD operation.

It can be clearly seen that when the converter is operating using the AGDs, the junction temperature T_j variations are reduced and the temperature trend is to be kept more constant.

According to the obtained lifetime results which are given in Table 4-1, the AGD strategy operation (compared with the TGD operation) has a positive impact of three times (for Denmark MP) to four times (for US MP) in improving the PV-inverter devices lifetime.



(a) Thermal loading of PV-inverter devices for one year operation in soft-environment conditions (Denmark-Aalborg)



(b) Thermal loading of PV-inverter devices for one year operation in harsh-environment conditions (USA-Arizona)

Figure 4-12 The thermal loading (mean junction temperature T_j) of PV-inverter devices which considers the traditional gate-driver and the advanced gate-driver strategy for one year operation in Denmark (a) and in USA (b).

Furthermore, it can be seen that the device lifetime is 75 % lower if the converter is operating in USA when compared to Denmark.

Finally, it can be concluded that the proposed ADs operation (compared with the traditional driving operation) has a positive impact in improving PV-inverter devices lifetime.

Table 4-1 The advanced gate-driver control-strategy impact in PV-inverter devices lifetime improvement

RFMP	Lifetime with degradation		AGD impact in lifetime	MP-variation (from Denmark to USA) impact in Lifetime for AD op.
	TGD operation	AGD operation		
U.S.A.	4.2 [years]	16,8 [years]	4X	75 [%]
Denmark	14 [years]	42 [years]	3X	

4.6 Summary

In this chapter a novel gate-driver concept has been introduced. An implementation and also a validation of the proposed advanced gate-driver have been achieved.

Based on the advanced gate-driver, a new method of active-thermal device control has been proposed, developed and validated. Moreover this chapter also proposes a novel advanced gate-driver control-strategy in order to improve the reliability of the PV-inverter devices. To proof the concept, the hardware implementation of the proposed advanced gate-driver has been done.

The proposed reliability oriented design tool has been used to study and evaluate the impact in PV-inverter devices lifetime of the proposed AGDs.

According to the obtained results, by using the advanced gate-driver strategy the lifetime of the PV-inverter devices is up to four times improved when compared to the traditional gate-driver.

Chapter 5

Conclusions and Future Work

The main conclusions of the thesis are underlined in this chapter along with several recommendations for future work regarding areas that could be further investigated.

5.1 Summary of Conclusions

To overcome the emerging challenges described in Chapter 1, the work developed during the Ph.D. studies is divided to cover two main topics: to develop a reliability-oriented design tool which is using a real-field mission-profile as input and also an advanced-GD for enhancing the reliability of power electronics devices.

The first part of the thesis focuses on the proposed reliability tool and it is presented in Chapter 2 and Chapter 3. In this part the modeling process of the tool is introduced. Therefore, a detailed description of the following models is presented: the real field mission profile model (developed based on the real field measurements for soft and harsh environment operating conditions for a PV-application), a grid connected PV-inverter model, the device electro-thermal modeling, and a lifetime model to assess the results. Moreover, the electro-thermal model validation has also been achieved for device level and system level operation.

Afterwards, a translation of the real field mission-profile to the device level thermal loading for one-year operation has also been done by developing the long term simulation model.

By taking the advantage of the main opportunities offered by WBG-devices, as a study case is proposed and implemented a SiC-based PV-inverter cost competitive with a Si-based one.

The second part introduces also a novel concept to assess the device reliability by considering the impact of the real field operating conditions

and also the device degradation.

The proposed reliability oriented design tool has been developed and used to perform complex lifetime analyses. Based on the obtained results it can be concluded that the main factors which have a negative impact on the lifetime-estimation accuracy of the power devices are: the impact of the device-degradation, the impact of the mission profile variation from soft to harsh environmental operating conditions, the impact of gate-driver parameters variation and the impact of the mission-profile sampling time. Finally, the proposed tool can provide information about how much each of the above mentioned factors affects the lifetime of the devices.

The second part of the thesis, which is presented in Chapter 4, studies an advanced gate-driver for enhancing the reliability of power electronics devices. In this context, a novel gate-driver concept which reduces the dependency of the device power losses variations on the device loading variations is developed.

In order to keep constant device power losses (implicitly also a constant device temperature), the proposed advanced gate-driver is able dynamically and accurately of controlling the gate-resistance and gate-voltage. Moreover, relying on the advanced-GD concept, an active-thermal control method for the device has been proposed and also validated. In order to validate the concept, a hardware implementation of the proposed advanced gate-driver has been done demonstrating the active thermal control.

Moreover, a novel advance gate-driver control-strategy for reliability improvement of the PV-inverter devices has been introduced. To evaluate the impact of the advanced gate-driver control-strategy in the PV-inverter devices lifetime, the proposed reliability oriented design tool has been used into the studies.

According to the obtained results, by using the advanced GD control-strategy, the lifetime of the PV-inverter devices may be considerably improved.

5.2 Contributions from the Authors Point of View

The main contributions of the thesis seen from the authors' point of view are summarized as follows:

Developed a novel reliability oriented design tool for the next generation of power converters which can be used in renewable energy systems.

- Developed and validated a novel Electro-Thermal model for SiC devices: device-level validation and converter-level validation
- Developed a Long Term Simulation Model (LTSM) which enables the translation of the real field mission profile operating conditions to the device level thermal loading within a reasonable framework of simulation time and accuracy.

Developed a novel gate-driver concept for enhancing the reliability of power electronics devices:

- Developed and validated an advanced gate-driver which is able dynamically and accurately to control the gate-resistance and gate-voltage in order to preserve a constant device loss dissipation, independent of the load variation.
- Proposed and developed advanced gate-driver strategy for improving the reliability of the converter devices.

The proposed reliability oriented design tool introduces a novel concept of assessing the reliability of power semiconductor devices by considering the device degradation related to the real field operating conditions. The tool has been used to perform the following reliability studies:

- Evaluated the impact of the long term mission-profile variation (from soft to harsh environmental operating conditions) and device degradation-aging in PV-inverter devices lifetime
- Evaluated the impact of the long term mission-profile variation and gate-driver parameters variation in the life-time of the converter devices.
- Evaluated the impact of the mission-profile sampling time in the lifetime-estimation accuracy. Determine the optimum sampling time as a compromise between lifetime-accuracy and simulation time.

- Evaluated the impact of the proposed active thermal control by using the advance gate-driver strategy in the PV-inverter devices lifetime.

5.3 Future work

The possibility for further improvement of the work can advance in to several directions. The main lines of research areas that could be of interest for the further investigation are as follows:

- The proposed reliability oriented design tool can be adapted to different topologies and applications (wind-turbine, pump, automotive, etc.). Minor modifications are required in respect to the mission-profile.
- Build a power cycling test setup (to perform accelerating lifetime tests) in order to develop specific lifetime models for the studied devices. In this way, by applying the proposed tool, more relevant and accurate results may be obtained.
- Perform an experimental validation of the thermal stress by measuring the device junction temperature and compare it with the estimated one by the proposed model. Determine the model accuracy.
- Introduce into the tool the lifetime estimation of the passive components (e.g. capacitors).
- Extend the lifetime models of the tool by taking into consideration also other stressors (e.g vibration, humidity, etc.).
- Perform an optimized design of the power converter by defining a relationship between the required converter lifetime and cost.
- Validate the degradation model.
- Perform more prototyping of the advanced gate-driver to see benefits of the performance

Bibliography

- [1] J. Arrillaga and N. Watson, Power System Harmonics. Wiley, 2003.
- [2] B.J Baliga, Silicon Carbide Power Devices. World Scientific Publishing Co. Pte. Ltd. 2006.
- [3] E.R. Brown, "Megawatt solid-state electronics", Solid-State Electronics, vol. 42, issue 12, pp. 2119-2130, December 1998.
- [4] B. Ozpineci, L.M. Tolbert, "Comparison of Wide-Bandgap semiconductors for Power Electronics Applications", US Department of Energy-Oak Ridge National Laboratory, December 12, 2003.
- [5] M. Shen, S. Krishnamurthy, M. Mudholkar, "Design and Performance of a High Frequency Silicon Carbide Inverter", IEEE Proc. of ECCE, pp. 2044-2049, 2011.
- [6] M. Hudson, R. Behnke, R. West, S. Gonzalez, J. Ginn, "Design Considerations for Three-Phase Grid Connected Photovoltaic Inverters", IEEE Photovoltaic Specialists Conference, pp.1396-1401, 2002.
- [7] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high power electronics," IEEE Transactions on Electron Devices, vol. 36, no. 9, pp. 1811-1823, 1989.
- [8] Y. Liu, Power Electronics Packaging, ISBN 978-1-4614-1052-2, Springer, 2012.
- [9] Website of International Conference on Silicon Carbide and related Materials, October 5-10, 2003.
- [10] W. Shockley, "Introductory Remarks in Silicon Carbide, A High Temperature Semiconductor", Pergamon Press, 1960.
- [11] <http://www.cree.com/news-and-events/cree-news/press-releases/2012/august/150mm-wafers>
- [12] B. Jeffrey, "SiC Power Devices and Modules Maturing Rapidly", Power Electronics Europe, Issue 1, 2013.
- [13] B. Callanan and J. Rice, "SiC MOSFETs under High-Frequency Hard Switched Conditions," Power Electronics Europe, Issue 4, 2012.
- [14] G. Deboy, R Rupp Infineon Technologies Austria/Germany, and R. Mallwitz, H. Ludwing, SMA Solar Technology Germany "New SiC JFET Boost Performance of Solar Inverters", Power Electronics Europe, Issue 4, 2011.
- [15] H. Neuenstein, J. Siemer, "Another A+," The Solar Power Magazine-Photon International, July 2012.
- [16] J. Lutz, "Packaging and Reliability of Power Modules", Proc. of IEEE International Conference on Integrated Power Systems (CIPS), pp. 1 – 8, 2014.
- [17] Ch. Herold, M. Schäfer, F. Sauerland, T. Poller, J. Lutz, O. Schilling, "Power cycling capability of Modules with SiC-Diodes", Proc. of IEEE

- International Conference on Integrated Power Systems (CIPS), pp. 1 – 6, 2014.
- [18] W. E. Newell, “Power electronics—Emerging from limbo,” *IEEE Trans. Ind. Appl.*, vol. 10, no. 1, pp. 7–11, Jan. 1974.
- [19] H. Wang, M. Liserre, F. Blaabjerg, P. de P. Rikken, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, “Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97-114, 2014.
- [20] P. Wikstrom, L. A. Terens, and H. Kobi, “Reliability, availability, and maintainability of high-power variable-speed drive systems,” *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 231–241, 2000.
- [21] H. Wang, K. Ma, and F. Blaabjerg, “Design for reliability of power electronic systems,” in *Proc. 38th IEEE Int. Conf. Ind. Electron.*, pp. 33–44, 2012.
- [22] L. M. Moore and H. N. Post, “Five years of operating experience at a large, utility-scale photovoltaic generating plant,” *J. Prog. Photovoltaic Res. Appl.*, vol. 16, no. 3, pp. 249–259, 2008.
- [23] F. Chan, H. Calleja, and E. Martinez, “Grid connected PV systems: A reliability-based comparison,” in *Proc. IEEE Int. Symp. Ind. Electron.*, pp. 1583–1588, 2006.
- [24] Y. Song and B. Wang, “Survey on reliability of power electronic systems”, *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013.
- [25] ZVEL, *Handbook for Robustness validation of automotive electrical/electronic modules*, June 2008.
- [26] E. Wolfgang, “Examples of failures in power electronics systems”, *ECPE Tutorial-Reliability of Power Electronics Systems*, Nuremberg, Germany, April 2007.
- [27] S.E. De Leon-Aldaco, H. Calleja, F. Chan, H.R. Jimenez-Grajales, “Effect of the mission profile on the reliability of a power converter aimed at photovoltaic applications—a case study”, *IEEE Trans. Power Electron.* vol. 28 no. 6, pp. 2998-3007, June 2013.
- [28] F. Chan, and H. Calleja, “Reliability estimation of three single-phase topologies in grid-connected PV systems”, *IEEE Trans. Ind. Electron.* vol. 58 no. 7, pp. 2683-2689, July 2011.
- [29] G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary, and M. Vitelli, “Reliability issues in photovoltaic power processing systems”, *IEEE Trans. Ind. Electron.* vol. 55 no. 7, pp. 2569-2580, July 2008.
- [30] S. E. De Leon-Aldaco, H. Calleja, F. Chan, and H. R. Jimenez-Grajales, “Effect of the mission profile on the reliability of a power converter aimed at photovoltaic applications—a case study,” *IEEE Trans. Power Electron.*, vol. 28 no. 6, pp. 2998–3007, Jun. 2013.
- [31] M. Ciappa, “Selected failure mechanisms of modern power modules,” *Microelectronics Reliability*, vol. 42, pp. 653–667, 2002.
- [32] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, “Fast power cycling test for IGBT modules in traction application,” in

- International Conference on Power Electronics and Drive Systems, vol. 1, pp. 425–430, 1997.
- [33] A. T. Bryant, P. A. Mawby, and P. R. Palmer, “Exploration of power device reliability using compact device models and fast electrothermal simulation,” *IEEE Transactions on Industry Applications*, vol. 44, no. 3, pp. 894–903, June 2008.
 - [34] D. Hirschmann, D. Tissen, S. Schrder, and R. Doncker, “Reliability prediction for inverters in hybrid electrical vehicles,” *IEEE Transactions on Power Electronics*, vol. 22, pp. 2511–2517, 2007.
 - [35] J. Gu and M. Pecht, “Predicting the Reliability of Electronic Products”, in *Proc. IEEE 8th International Conference on Electronic Packaging Technology ICEPT*, pp. 1-8, 2007.
 - [36] H. Huang, P.A. Mawby, “A Lifetime Estimation Technique for Voltage Source Inverters”, *IEEE Trans. on Power Electron.*, vol. 28 no. 8, pp. 4113-4119, Aug. 2013.
 - [37] D. Hirschmann, D. Tissen, S. Schrder, and R. Doncker, “Inverter design for hybrid electrical vehicles considering mission profiles,” in *Proc. IEEE Vehicle Power and Propulsion*, pp. 567-573, 2005.
 - [38] K. Ma, M. Liserre, F. Blaabjerg, “Lifetime Estimation for the Power Device Considering Mission Profiles in Wind Power Converter”, in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2962-2971, Sep. 2013.
 - [39] Y. Yang, H. Wang, K. Ma, F. Blaabjerg, “Mission profile based multi-disciplinary analysis of power modules in single-phase transformerless photovoltaic inverters”, *Proc. IEEE Power Electronics and Applications (EPE)*, pp. 1-10, 2013.
 - [40] D. Zhou, F. Blaabjerg, M. Lau, M. Tonnes, “Thermal Behavior Optimization in Multi-MW Wind Power Converter by Reactive Power Circulation”, *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 433-440, 2013.
 - [41] D. A. Murdock, J. E. Torres, J. Connors, and R. D. Lorenz, “Active Thermal Control of Power Electronic Modules”, *IEEE Transactions on Industry Applications*, vol. 42, no. 2, pp. 552-558, 2006.
 - [42] K. Ma, M. Liserre, F. Blaabjerg, “Reactive Power Influence on the Thermal Cycling of Multi-MW Wind Power Inverter,” *IEEE Trans. on Industry Applications*, vol. 49, no. 2, pp. 922-930, 2013.
 - [43] Y. Yang, H. Wang, F. Blaabjerg, “Reactive Power Injection Strategies for Single-Phase Photovoltaic Systems Considering Grid Requirements”, *IEEE Transactions on Industry Applications*, Vol. 50, No. 6, pp. 4065-4076, 2014.
 - [44] Y. Xue, K.C. Divya, G. Griepentrog, M. Liviu, S. Suresh, and M. Manjrekar, “Towards next generation photovoltaic inverters”, *IEEE ECCE*, pp. 2467-2474, 2011.
 - [45] F. Blaabjerg, R. Teodorescu, M. Liserre and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 1398-1409, 2006.

- [46] A.Luna, J. Rocabert, G. Vazquez, P. Rodriguez, R. Teodorescu and F. Corcoles, "Grid synchronization for advanced power processing and FACTS in wind power systems," in *Industrial Electronics (ISIE)*, 2010 IEEE International Symposium on, pp. 2915-2920, 2010.
- [47] R. Teodorescu, M. Liserre and P. Rodriguez, *Grid Connected Converters for Photovoltaic and Wind Power Systems*. Wiley, 2011.
- [48] A. Mir, C. Sintamarean, H. Beltran, "Control of a Three-Level Converter for Power Quality Improvement in Wind Power Plants," *IEEE International Symposium on Industrial Electronics (ISIE)*, pp.2026-2031, July 2012.
- [49] E. Fred Schubert, *Light-Emitting Diodes Second Edition*, Cambridge University Press, ISBN 978-0-521-86538-8, 2006.
- [50] Texas Instruments application note: "Estimating MOSFET Parameters from the Data Sheet", <http://www.ti.com/lit/ml/slup170/slup170.pdf>
- [51] R. Singh et al, "Reliability of SiC MOS devices", *Solid State Electronics*, 48, pp. 1717-1720, 2004.
- [52] A. K. Agarwal et al, "Temperature Dependence of Fowler-Nordheim Current in 6H- and 4H-SiC MOS Capacitors" *IEEE Electron Device Lett.*, pp. 592-594, 1997.
- [53] M. M. Maranowski et al, "Time-Dependent-Dielectric-Breakdown Measurements of Thermal Oxides on N-Type 6HSiC", *IEEE Trans. Electron Devices*, pp. 520-524, 1999.
- [54] K. Matocha et al, "Time-Dependent Dielectric Breakdown of Neep Thermal Oxides on 4H-SiC", *Materials Science Forum Vols. veep 556-557*, pp. 675-678, 2007.
- [55] Y. Liangchun, K.P. Cheung, J. Campbell, J.S. Suehle, K. Sheng, "Oxide Reliability of SiC MOS Devices", *IEEE International Integrated Reliability Workshop Final Report*, pp. 141-144, 2008.
- [56] A. Scott, "Silicon Carbide MOSFETs for High Powering Modules", *APEC-tutorial*, 2013.
- [57] M. Ciappa, "Selected failure mechanisms of modern power modules", *Microelectron. Reliab.*, vol. 42, pp. 653-667, 2002.
- [58] R. Bayerer, T. Hermann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules various factors influencing lifetime," in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, pp. 1-6, Mar. 2008.
- [59] U. Scheuermann and U. Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," in *Proc. PCIM Nuremberg*, pp. 59-64, 2002.
- [60] W. W. Lee, L. T. Nguyen, and G. S. Selvaduray, "Solder joint fatigue models: Review and applicability to chip scale packages," *Microelectron. Reliab.*, vol. 40, pp. 231-244, 2000.
- [61] M. Held, P. Jacob, G. Nicoletti, and P. Scacco, "Fast power cycling test for IGBT modules in traction application," *Proc. Int. Conf. Power Electron. Drive Syst.*, vol. 1, pp. 425-430, 1997.

- [62] U. Scheuermann and U. Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," in Proc. PCIM Nuremberg, pp. 59–64, 2002.
- [63] ECPE Workshop 'Lifetime Modelling and Simulation', Dusseldorf, Germany, July 03-04, 2013.
- [64] M. A. Miner, "Cumulative damage in fatigue," Journal of Applied Mechanics, no. 12, pp. 159-164, 1945.
- [65] M. Musallam and C.M. Johnson, "An efficient implementation of the rainflow counting algorithm for life consumption estimation," IEEE Trans. Reliability, vol. 61, no. 4, pp. 978–986, Dec. 2012.
- [66] Y. Kim, H. Cha, B. Song, Y. Lee, "Design and Control of a Grid-Connected Three-Phase 3-Level NPC Inverter for Building Integrated Photovoltaic Systems", Proc. of IEEE Innovative Smart Grid Technologies (ISGT), pp. 1-7, 2011.
- [67] M. Hudson, R. Behnke, R. West, S. Gonzalez, J. Ginn, "Design Considerations for Three-Phase Grid Connected Photovoltaic Inverters", Proc of IEEE Photovoltaic Specialists Conference, pp.1396-1401, 2002.
- [68] H. Preckwinkel, D. Krishna, N. Fröhleke, J. Böcker, "Photovoltaic Inverter with High Efficiency over a Wide Operation Area – A Practical Approach", Proc. of IECON, pp.912-917, 2011.
- [69] F. Blaabjerg, K. Ma and D. Zhou, "Power electronics and reliability in renewable energy systems", Proc. of IEEE International Symposium on Industrial Electronics (ISIE), pp. 19-30, July 2012.
- [70] M. Hudson, R. Behnke, R. West, S. Gonzalez, J. Ginn, "Design Considerations for Three-Phase Grid Connected Photovoltaic Inverters", Proc. of IEEE Photovoltaic Specialists Conference, pp.1396-1401, 2002.
- [71] H. Wang, H. Chung, W. Liu, F. Blaabjerg, "Long lifetime DC-link voltage stabilization module for smart grid application", Advances in Power System Control, Operation and Management (APSCOM 2012), 9th IET International Conference, pp. 1-6, 2012.

PART II - Publications

Publication I

C. Sintamarean, F. Blaabjerg, H. Wang and Y. Yang, “Real Field Mission Profile Oriented Design of a SiC-Based PV-Inverter Application”, IEEE Transactions on Industry Applications, Vol. 50, no 6, pp. 4082-4089.

Publication year: 2014.

Publication II

C. Sintamarean, F. Blaabjerg, H. Wang and P. De P. Rikken, “A design tool to study the impact of mission-profile on the reliability of SiC-based PV-inverter devices”, ESREF-Microelectronics Reliability, pp. 1655-1660.

Publication year: 2014.

Publication III

C. Sintamarean, F. Blaabjerg, H. Wang F. Iannuzzo and P. De P. Rimmen, “Reliability Oriented Design Tool for the New Generation of Grid Connected PV-Inverters”, IEEE Transactions on Power Electronics-Special Issue in Reliability, Vol. 30, no. 5, pp. 2635-2644.

Publication year: 2015.

Publication IV

C. Sintamarean, F. Blaabjerg, and H. Wang, "A Novel Electro-Thermal Model for Wide Bandgap WBG-semiconductor based devices", Proceedings of IEEE 15th European Conference on Power Electronics and Applications (EPE –ECCE Europe), pp. 1-10.

Publication year: 2013.

Publication V

C. Sintamarean, F. Blaabjerg, and H. Wang, "Comprehensive Evaluation on Efficiency and Thermal Loading of Associated Si and SiC based PV Inverter Applications", Proceedings of IEEE 39th Industrial Electronics Society (IECON) , pp. 555-560.

Publication year: 2013.

Publication VI

C. Sintamarean, F. Blaabjerg, H. Wang and Y. Yang, “Real Field Mission Profile Oriented Design of a SiC-Based PV-Inverter application”, Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE), pp. 940-947,

Publication year: 2013.

Publication VII

C. Sintamarean, E. Eni, F. Blaabjerg, R. Teodorescu, and H. Wang, "Wide band-gap devices in PV systems-opportunities and challenges", Proceedings of IEEE International Power Electronics Conference (IPEC-ECCE Asia), pp. 1912-1919.

Publication year: 2014.

Publication VIII

C. Sintamarean, F. Blaabjerg, H. Wang and F. Iannuzzo, “The Impact of Gate-Driver Parameters Variation and Device Degradation in the PV-Inverter Lifetime”, Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2257-2264.

Publication year: 2014.

